INTEGRATION, the VLSI journal xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Transceiver design for LVSTL signal interface with a low power on-chip self calibration scheme

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ARTICLE INFO

Keywords:
DRAM chips
CMOS transceiver circuit
LVSTL
LPDDR4
Driver circuits
Impedance calibration
Random access memory
I/O interface
On-chip sensor
Temperature sensor
Process sensor
Self-calibration
Adaptive gain control (AGC)

ABSTRACT

An on-chip impedance self calibration methodology for LVSTL (low voltage swing termination logic) for LPDDR4 (low power double data rate) application is proposed. The proposed calibration is to compensate mismatches and variations of the transmitter output drivers due to process and temperature variations. The impedance matching concept uses process sensor and temperature monitoring sensors closely located to DQ pins as a means to detect and compensate the transistor mismatches of the output driver due to process and temperature variations. The proposed circuitry is designed with DRAM bidirectional transceiver and implemented using a 180 nm CMOS technology, and the impedance calibration technique is demonstrated with various external termination resistance of 40/48/60/80/120/240 Ω. In the receiver end, a PMOS input sense amplifier is designed considering the required common mode range for the LVSTL signal interface, and an adaptive gain control scheme is also applied on the receiver design. The process sensor is utilized to adaptively control the gain factor of the receiver. The active area including power-ring of the transmitter is 0.48 mm^2 with 0.14 mm^2 of the proposed calibration circuit. Since there are 32 transceivers for two channels and the channels share the calibration circuits on the same DRAM die, the area overhead is less than 1.5%. The power consumption of the calibration circuits is 160 μW with 1.8 V power supply at 180 nm CMOS technology node.

1. Introduction

Bandwidth of mobile DRAM has been continuously increased from generation to generation as the amount of data transmission rapidly increases along with the processing contents such as high-resolution display as well as high speed wireless communications [1,2]. In the meantime, the growth of mobile device demand makes not only performance but also battery lifetime critical factors, which makes power consumption issue even more critical and many power reducing techniques are being used [3–5]. However, in mobile application, number of I/O pins is increased as a solution to extend data bandwidth. Therefore, I/O part still takes a large portion in the power consumption.

To satisfy fast memory operating speed and low power consumption requirements, the low voltage swing termination logic (LVSTL) interface is standardized [6] from the 4th generation (LPDDR4) in mobile applications. The LVSTL interface has advantages of low C_{io} (input/output capacitance) and low power consumption with lowered output swing level (VOH) and no static power consumption while driving logic low.

With the low voltage signal swing, the signal integrity in transmitting and receiving the signal becomes more important along with the data transmitting speed. Since the serial interface between two different digital systems with communication channel is limited by the bandwidth, not only those problems caused by switching noise or crosstalk but also signal attenuation or reflection problems caused by impedance mismatching in high frequency operation become challenging issues. The problems are exacerbated at the low power application, where the VOH is scaled down to VDDQ/3 in the low power DDR standard as shown in Fig. 1. In addition, process and temperature variations as wells as device mismatches are critical factors that make it difficult to accomplish uniform device parameters and performances. Furthermore, thermal issue is also a major issue not only in the currently used LPDDR4 standard but also in other systems beyond this configuration including wide I/O signal transmission. The thermal drift has a high correlation with refresh timing control of the output driver training that is also a major concern to ensure reliable system operation and achieve high data rate [7]. Therefore, transceiver design with high sensitivity as wells as proper training sequences is required to achieve high quality of signal integrity. Several I/O training operations have been used and additional constraints are included in DRAM operation

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https://doi.org/10.1016/j.vlsi.2018.06.006
Received 2 March 2018; Received in revised form 14 May 2018; Accepted 26 June 2018

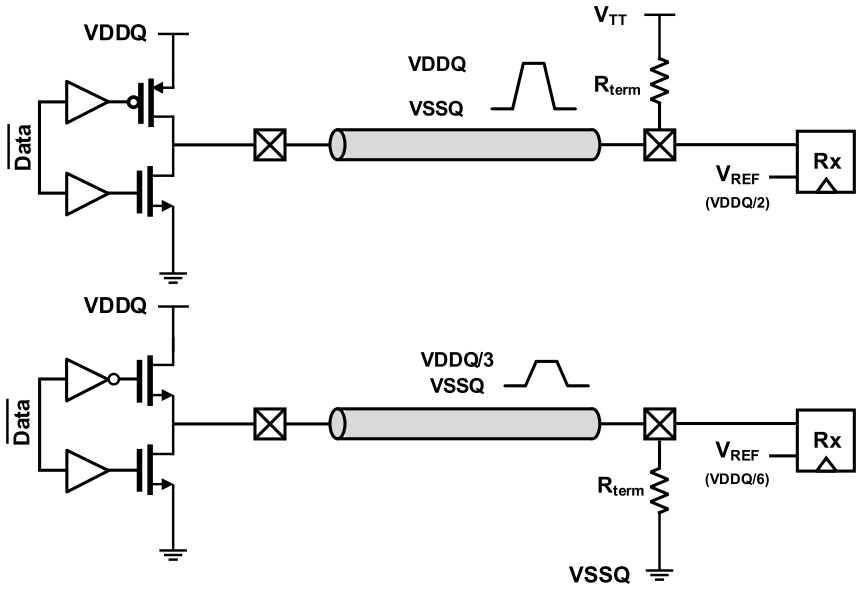

Fig. 1. VDDQ and low voltage swing with VSSQ termination.

to achieve high data bandwidth and low BER. Training for CA (Calibration for Command Address), and VREF (Reference Voltage Calibration) are such operations for proper signal transmission. Also, ODT (On-Die Termination) reduces electrical discontinuity introduced from off-die termination for high-speed operation. ZQ calibration (impedance calibration for output driver) is one of the DRAM feature that allows DRAM to match driver impedance characteristics to termination resistor for each DQ (Data Input/Output pin). Currently, most of the conventional output driver calibration schemes use the ZQ pin and on-chip resistor RZQ to compensate impedance mismatches [4,8–11]. However, designs of the conventional methods are very complex and it is hard to achieve high precision of accuracy at a reasonable area and power overhead. The digital circuits including decoder and digital filters of the conventional calibration system take large circuit area in Ref. [8]. In Ref. [9], the calibration cycles for every DQ and DQS pins still remain within long operation cycles, and the calibration is performed in parallel for every DQ pins in Ref. [10]. These existing methods consume high power due to the ring counter and control circuit that operate at high frequency. Furthermore, the conventional methods do not provide the adaptive or self-calibration feature against process and temperature variations. This is a critical drawback as the latest nanoscale transistors are very sensitive to process and temperature variations.

As an efficient solution of the aforementioned issues, we propose an on-chip variation aware open-loop self-calibration method to compensate offsets and improve the performance of the interface circuits. The open-loop technique provides much smaller yet faster calibration method, and it consumes less power than the conventional feedback calibrations with trade-off on inaccuracy. Another advantage is that timing burden and complexity of design are significantly reduced comparing to the conventional methods while preventing performance degradation from process variations and temperature drift. To demonstrate the feasibility of the method, we propose an on-chip impedance open-loop calibration technique to actively control the characteristics of the transmitter output drivers. In addition, a low common mode voltage in receiver is inevitable in the LVSTL interface. Therefore, PMOS input sense amplifier is designed for the receiver considering the low common mode range. The input MOSFETs are designed with a set of array to provide an adaptive gain control feature to compensate process and temperature variation, which makes it possible to accomplish performance optimization and low power consumption.

The output driver calibration approaches are outlined in Section 2 including the proposed calibration scheme that uses on-chip process sensor and temperature monitoring sensor. Section 3 discusses the design methodology on LVSTL transceiver including an area efficient output driver design for transmitter with ESD protection resistors. The adaptive gain controlled (AGC) PMOS input sense amplifier, process sensor, and temperature monitoring sensor designs are analyzed in Section 3. The measured data are presented in Section 4, followed by the conclusion in Section 5.

2. On-chip output driver calibration

2.1. Conventional approach

A conventional ZQ calibration for DRAM transmitter is exemplified in Fig. 2. One pull-up unit is composed of an n-bit pull-up transistor array to set 240 Ω pull-up driver. There are 6 units connected in parallel for different termination impedance matching cases, and pull-down driver is constructed in the same manner. When the ZQ command is launched, pull-down driver is trimmed first without pull-up transistors (switch 2 in Fig. 2 is open at this time). The pull-down transistors are all turned off initially and the DQ node is connected to VDDQ through 240 Ω external resistor, and the DQ node voltage is compared with VDDQ/2. The calibration continues by turning the pull-down transistors one by one from LSB until the comparator detects that DQ node is low. The next step is to set VOH level from pull-up driver calibration. In this step, one of the comparator inputs is switched to VOH, and the driving strength of the pull-up driver is adjusted in the same way as the pull-down driver. The main drawback of the conventional approach is that the calibration has to be performed sequentially for each of the units and each of DQ pins due to the voltage and temperature drift.

2.2. Proposed on-chip output driver calibration with on-chip variation sensing

The current LPDDR4 DRAM-Soc/AP interface requires two channels on one die and each channel has total 16 I/O (DQ) pins, and there are total 32 DQ pins on the same die. Fig. 3 illustrates the proposed on-chip calibration technique at the interface between DRAM and SoC/AP application for the half DQ pins of the channel in LPDDR4 architecture. The proposed impedance calibration method compensates impedance mismatches from process and local temperature variations [12]. One process sensor is located on the die, and two localized temperature-monitoring sensors are placed close to the 8 DQ pins to increase sensing