INTEGRATION, the VLSI journal xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

A 1.5 ~ 5 GHz CMOS broadband low-power high-efficiency power amplifier for wireless communications

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ARTICLE INFO

Keywords:
Word
Ultra-wideband
Power amplifier
PA
Low-power
CMOS

ABSTRACT

This paper describes the design of 1.5–5 GHz CMOS power amplifier (PA) for broadband applications that uses 0.18-μm CMOS technology. This UWB PA uses a cascode topology with current-reuse, to enhance the gain at the upper end of the desired band, and a resistive feedback amplifier stage to achieve optimum output power and gain while maintaining a wide bandwidth. The measured results for the proposed UWB PA show an excellent gain in flatness of 20 ± 1 dB over the 2.0–4.0 GHz frequency range. The average gain is about 17.8 dB from 1.5 to 5 GHz. The reverse isolation is less than −42 dBm. The PA has an efficiency of a maximum of 30.5% at 2 GHz, 24.8% at 3 GHz, 28.1% at 4 GHz and 15.2% at 5 GHz with a 50 Ω load termination. The amplifier delivers a P_{1dB} output power of 6.7 dBm and a PAE of 22% at 4 GHz is obtained with a power consumption of 24.5 mW from a 1.8 V supply voltage. The chip area is 1.222 × 1.004 mm^2, including the pads. The proposed UWB PA exhibits high gain and is highly efficient. It has the highest FOM for power amplifiers in the 2–6 GHz band.

1. Introduction

In recent years, wireless connection has become common in new communication systems, and demand for high-data-rate wireless communications is increasing. Some of the wireless personal communications have to be portable and they require low power single-chip radio-frequency transceiver front-end in order to increase the battery life. The Wireless LAN (IEEE 802.11b/IEEE 802.11g), Bluetooth, Wireless sensor, and ZigBee networks work in the 2.4 GHz band [1]. For wireless personal area network (WPAN) applications, the UWB communication system is widely used in short distance wireless local area networks, because it allows a wide band and high bit rates. The IEEE 802.15.3a Ultra-Wideband (UWB) system uses a specific frequency band (3.1 GHz–10.6 GHz) to access data and uses orthogonal frequency-division multiplexing (OFDM) modulation [2–5]. The system operates across a wide range of frequency (3.1–10.6 GHz). The low-frequency band stretches from 3.1 to 4.8 GHz. Fig. 1 shows the band structure for UWB applications. The high-frequency band stretches from 6 to 10.6 GHz. UWB technology has possible applications in imaging systems, sensor networks, wireless personal area networks (WPAN) and biomedical electronics. The system has several advantages, such as low complexity, low cost and a high data rate for the wireless system.

This study designs a low-power direct-conversion Power Amplifier for an MB-OFDM UWB RF transmitter, as shown in Fig. 2. In the direct-conversion architecture circuit design, CMOS technology provides a single-chip solution, which greatly reduces the cost, and is widely used in UWB receivers. In the front–end system, a power amplifier is the last block in the transmitter path for a communication system. The power amplifiers are the most important core components in transmitter modules. The power amplifiers are the primary consumers of power supply among radio frequency blocks. The PA must achieve a high power added efficiency (PAE) value over the entire bandwidth, feature a flat gain and good linearity and have a small chip size and low power consumption. As the key circuit in transceiver, the most challenges of CMOS power amplifier (PA) design are poor linearity and low power-added efficiency (PAE) [6]. In radio frequency circuits, SiGe and GaAs transistors perform fairly well. However, these processes lead to increased cost and greater complexity. In this paper, a broadband CMOS power amplifier from 1.5 to 5 GHz for MB-OFDM UWB applications is presented. The proposed design only focuses on a high power added efficiency (PAE), bandwidth, linearity and the power consumption of the UWB PA. The PA topology is proposed in section 2. A complete analysis of the design methodology for the wideband matching network is presented in section 3. In section 4, the implementation and results are presented. The conclusion is presented in the last section.

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https://doi.org/10.1016/j.vlsi.2018.07.003
Received 9 February 2018; Received in revised form 30 May 2018; Accepted 10 July 2018

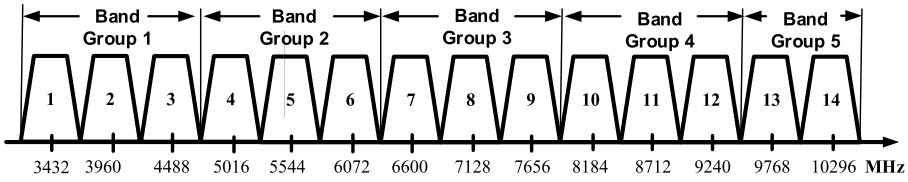

Fig. 1. The IEEE 802.15.3a frequency band.

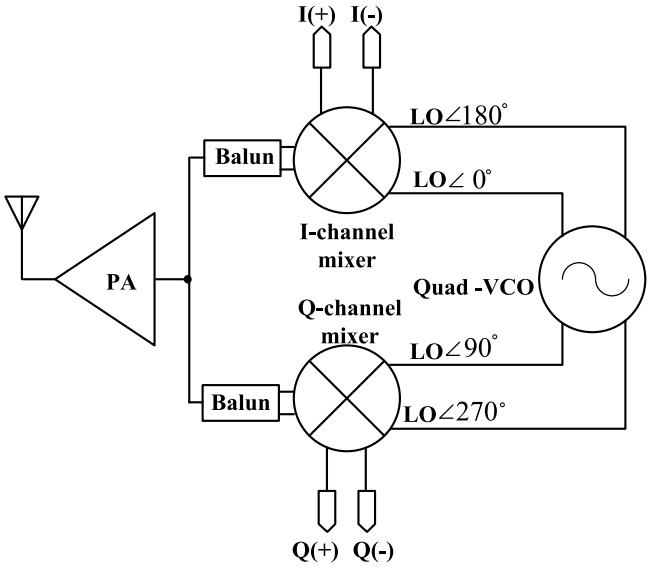

Fig. 2. A block diagram of the direct-conversion transmitter including the proposed PA.

2. PA circuit design and analysis

A conventional two-stage common-source amplifier design is depicted in Fig. 3(a). Fig. 3(b) illustrates a two-stage common-source amplifier with a current reuse topology [7–11]. To ensure low power consumption, the two-stage amplifier is folded into a single stage. The power consumption for a conventional two-stage DC amplifier is expressed as

$$P_{DC} = V_{DD} \times (I_{D1} + I_{D2}) \tag{1}$$

The current power consumption for a reuse topology DC amplifier is expressed as

$$P_{DC} = V_{DD} \times (I_D) \tag{2}$$

If the same gain performance is $I = I_D = I_{D1} = I_{D2}$, then for the same gain, this circuit only consumes about half the power of the two-stage amplifier. The current reuse topology PA shares the same supply current, to reduce power consumption. Fig. 4 shows the approximate equivalent small signal circuit for the current-reused amplifier. C_2 and M_2 provide a low impedance path without any dc current. The impedance of L_1 increases with frequency so there is a high impedance path to block the signal. At high frequencies, the current gain for the first stage is expressed as follows [8]:

$$\frac{i_{d2}}{i_{d1}} = \frac{g_{m1}}{s[C_{gs1} + C_{gd1} \times (K_1)]} * \frac{(K_1/sC_{gd1})//r_{o1}//sL_1}{[(K_1/sC_{gd1})//r_{o1}//sL_1 + R_{g2} + (1/sC_1)]} \tag{3}$$

where C_{gs1} is the gate-source capacitance, K_1 is the voltage gain, C_{gd1} is the gate to drain capacitance and r_o is the resistance of M_1 at the drain node, R_{g2} is the resistance of M_2 at the gate-source and g_{m1} is the transconductance of the input transistor, M_1.

$$[(K_1/sC_{gd1})//r_{o1}//sL_1] > > [R_{g2} + (1/sC_1)] \tag{4}$$

Therefore, $[(K_1/sC_{gd1})//r_{o1}//sL_1]$ provides a sufficiently high impedance along the signal path. The first stage current gain value is conservatively estimated as

$$\frac{i_{d2}}{i_{d1}} \approx \frac{g_{m1}}{s[C_{gs1} + C_{gd1} \times (K_1)]} \tag{5}$$

Using the same example, the current gain for the second stage is expressed as follows:

$$\frac{i_{d3}}{i_{d2}} = \frac{g_{m2}}{s[C_{gs2} + C_{gd2} \times (K_2)]} * \frac{(K_2/sC_{gd2})//r_{o2}}{[(K_2/sC_{gd2})//r_{o2} + sL_2]} \tag{6}$$

$$[(K_2/sC_{gd2})//r_{o2} > > sL_2] \tag{7}$$

The second stage current gain is conservatively estimated as:

$$\frac{i_{d3}}{i_{d2}} \approx \frac{g_{m2}}{s[C_{gs2} + C_{gd2} \times (K_2)]} \tag{8}$$

The current gain is conservatively estimated as:

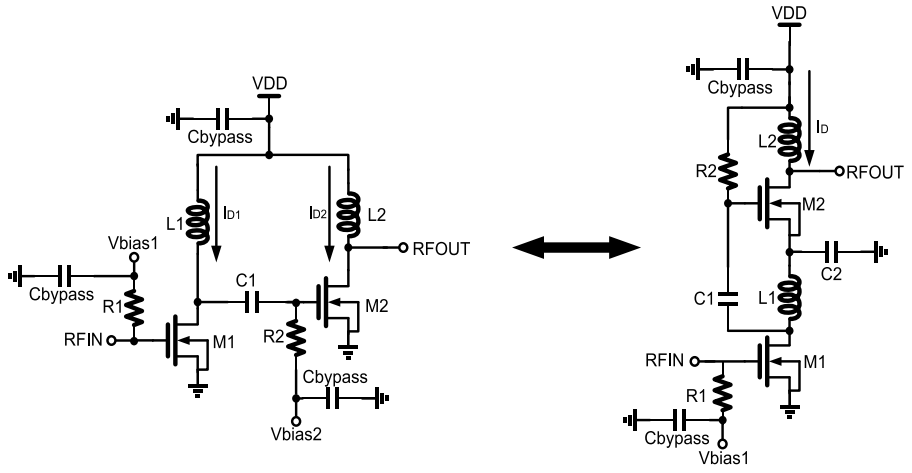

Fig. 3. (a) cascaded structure (b) current-reused structure.