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Super class AB-AB bulk-driven folded cascode OTA

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ABSTRACT

A super class AB-AB bulk-driven folded cascode operational transconductance amplifier (OTA) with improved slew rate and unity-gain bandwidth is presented. The proposed bulk-driven amplifier utilizes the adaptively biased circuits, the bulk-driven flipped voltage follower and quasi-floating gate circuit, to implement the class-AB input stage and class-AB output stage respectively, which provides enhanced unity-gain bandwidth and dynamic current boosting. The proposed bulk-driven OTA is simulated on the 0.18 μm SMIC process with 1 V low voltage supply. The simulation results show that the proposed class AB-AB bulk-driven OTA achieves the increased factor of 6.5 and 4.7 in unity-gain bandwidth and slew rate compared with that of conventional class-A counterpart with only 50% extra power consumption.

1. Introduction

With the electronic market trends to low-voltage and low-power, the bulk-driven (BD) operational transconductance amplifiers (OTAs) have been more popular than gate-driven OTAs due to the rail to rail operation [1,2]. In addition, the folded cascode (FC) structure is often applied in BD OTA because of its high gain and reasonably large signal swing [3,4]. However, the BD OTA has an obvious drawback due to the smaller bulk transconductance (g_{mb}) [5] which limits the improvement of unity-gain bandwidth (GBW) and dc gain [6,7]. Recently, some techniques including the positive feedback source degradation [8] and auxiliary differential pairs [9] have been applied to increase effective transconductance of the BD OTA, but these techniques do not mention the improvement of the slew rate (SR). Actually, the achievable maximum value of output current is restricted by the tail current of input pairs and the folded current source of output stage in the traditional bulk-driven folded cascode (BDFC) OTA, making it working at class-A status [10]. That is the fundamental reason for the constraint of the SR. Note that the bulk-driven transistor has poor current driven capability due to the small value of η [11,12]. To resolve this issue, it is considered to drive the folded current source transistor with a voltage variation.

In this paper, we present a super class AB-AB bulk-driven folded cascode (SBDFC) OTA with enhanced SR and GBW. Two bulk-driven flipped voltage followers (BFVFs) [11] are applied to achieve the class-AB input operation, improving the effective transconductance of SBDFC OTA. In addition, the quasi-floating gate (QFG) circuit [13–16] is utilized to drive the folded current source transistor in SBDFC OTA, forming the class-AB output stage which further enhances the effective transconductance and improves the maximum output current.

The following sections present the details of the proposed super class AB-AB bulk-driven folded cascode OTA. In Section 2, we summarize the primary performance of the traditional BDFC OTA. In Section 3, We analyze the circuit implement structure of our proposed SBDFC OTA. In section 4, the performance analysis of the proposed SBDFC OTA are discussed. The performance comparisons, the traditional BDFC OTA and the proposed SBDFC OTA, are given in the Section 5. The Section 6 gives the conclusions.

2. The traditional BDFC OTA

Fig. 1 shows the conventional class-A bulk-driven folded cascode OTA. The tailed current source transistor M_0 and folded current source transistor $M_{3,4}$ are all set to be $2I_B$. In quiescent condition, the total current of BDFC OTA is $4I_B$. Note that the equivalent transconductance (G_m) of traditional BDFC OTA can be expressed as,

$$G_{m,BDFC} = g_{mb1,2} \tag{1}$$

where $g_{mb1,2}$ is the bulk transconductance of input transistors $M_{1,2}$. Thus, the GBW of the traditional BDFC OTA can be given as,

$$GBW_{BDFC} = \frac{G_{m,BDFC}}{C_L} \tag{2}$$

In addition, the SR of the traditional BDFC OTA can be given as,

$$SR_{BDFC} = \frac{2I_B}{C_L} \tag{3}$$

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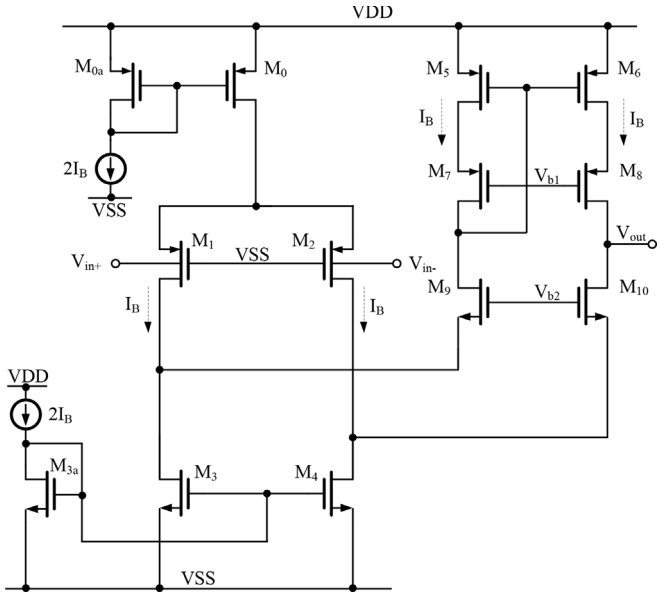


Fig. 1. The traditional class-A BDFC OTA.

As mentioned before, the achievable maximum output current is limited by the biased current I_B. Usually, the figure-of-merit (FoM) is used to evaluate the current efficiency (CE) of an OTA. Note that the FoM_S shows the small signal power ratio and is expressed as, $FoM_S = 100 \cdot GBW \cdot C_L/I_{supply}$. In addition, the FoM_L shows the large signal current efficiency and is expressed as, $FoM_L = SR \cdot C_L/I_{supply}$, where I_{supply} is the total current of each BD OTA. Therefore, the FoM value for BDFC can be given as,

$$FoM_{s,BDFC} = 100 \cdot \frac{g_{mb1,2}}{4I_B} \tag{4}$$

$$FoM_{s,BDFC} = \frac{2I_B}{4I_B} = 0.5 \tag{5}$$

Obviously, the CE of traditional BDFC OTA is not large enough.

3. The proposed SBDFC OTA

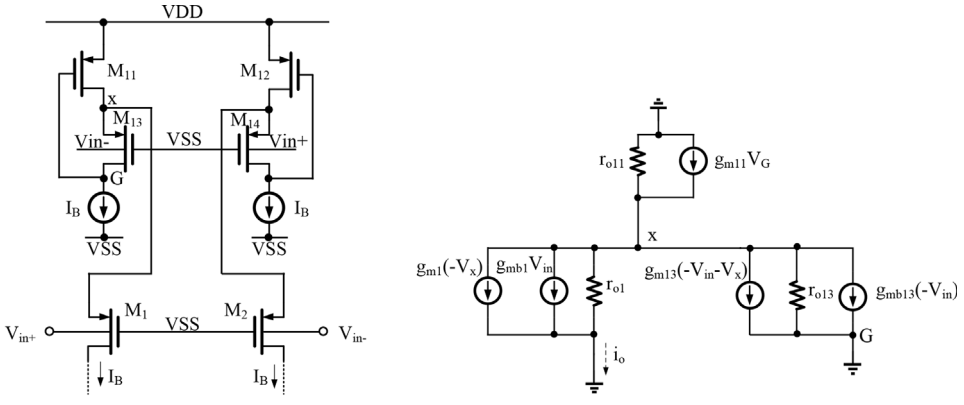
To overcome the shortcomings of traditional BDFC OTA, we proposed the adaptive biasing class-AB input stage and class-AB output stage to improve the equivalent transconductance and maximum output current of BDFC OTA. Figs. 2 and 3 show the proposed input stage and output stage of the SBDFC OTA, respectively.

3.1. Class AB input stage

Fig. 2a shows the proposed class-AB input stage of proposed class AB-AB SBDFC OTA. The two BFVFs are applied in input stage to achieve the class AB input stage. The BFVF is implemented by the diode-connected transistors $M_{11,12}$ [11,17], the BD transistor $M_{13,14}$ and the current source I_B. In quiescent condition, the current of input differential pairs is I_B which is equal to that of in BDFC OTA. Assuming that the V_{in+} is decreased, the source voltage of transistor M_{14} in BFVF is also decreased while that of M_1 remains constant. Thus the current of M_2 is decreased while that of M_1 is increased. These current in M_1 and M_2 is not limited by bias current source I_B to achieve the class AB input operation. Compared with conventional FC OTA, the differential input signal in proposed SBDFC OTA is not only applied in the bulk terminal of input differential transistors but also source terminal, making the effective transconductance become $2g_{mb1}$.

3.2. Class AB output stage

The BFVFs applied in input stage could double GBW but could not increased dynamic output current. Actually, the achievable dynamic output current is limited by the folded current source of output stage. To solve these issue, the QFG circuit structure is applied in output stage, as shown in Fig. 3. The capacitance C_1 and the transistor M_{R1} form the QFG circuit. Note that the diode-connected transistor M_{R1} is equivalent to the large resistor [13,16], and we chose that the diode connection of the PMOS transistor M_{R1} is established in between gate and drain, bulk and source, respectively. In quiescent condition, the current of transistor M_3 is accurately set to be $2I_B$, regardless of PVT variations. In addition, the gate of transistor M_{11} is connected to the gate of folded current source transistor M_3 through capacitance C_1. During the dynamic operation, when the input signal is slewing, the voltage at node A is subject to large change. Note that the capacitor C_1 can not charge or discharge rapidly so that it acts as a floating battery shown in Fig. 3a that transfers the voltage variations at node A to node B after attenuation by a factor of $C_1/(C_1 + C_B)$ [13–16]. Note that the C_B is the parasitic capacitance at the node B, and is approximately C_{gs3}. Considering the weak leakage current in the gate of transistor $M_{3,3a}$, the diode-connected transistor M_{R1} could work and act as the large resistance. Hence, the resistance M_{R1} and the capacitor C_1 form the first-order RC high-pass filtering. Due to the diode-connected transistor has the extremely high resistance value, the signal above 100 Hz could pass through the RC high-pass filtering [13,16]. Therefore, the voltage swing at the gate of M_{11} can transmit to the gate of transistors M_3 to generate the dynamic output current, achieving the class AB output operation.



(a) The proposed input stage of SBDFC OTA (b) The small-signal equivalent circuit of the input stage

Fig. 2. The proposed input stage of SBDFC OTA.