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NoC-DPR: A new simulation tool exploiting the Dynamic Partial Reconfiguration (DPR) on Network-on-Chip (NoC) based FPGA

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ABSTRACT

Due to the ability of Dynamic Partial Reconfiguration (DPR) of SRAM-based Field Programmable Gate Arrays (FPGAs) to add more flexibility over runtime phase, DPR is attracting more interest. Recently, FPGA manufacturers are facilitating the design of applications that utilize DPR. One of the main issues in our knowledge of DPR's current techniques (i.e., ICAP and JTAG) is a performance bottleneck; only one DPR is allowed at a time. In this paper, a state-of-art NoC-based FPGA simulator which supports DPR simulation is proposed. The proposed NoC-DPR simulator is used to investigate design limitations and performance degradation of using DPR on NoC-based FPGA. To estimate the reconfiguration time overhead, which results from increasing the number of simultaneous DPRs on FPGA fabric, some experimental investigations are carried out using NoC-DPR simulator. These investigations revealed that the overhead of reconfiguration time increases exponentially with increasing the number of simultaneous DPRs. However, further investigations show that the network of wormhole routers with virtual channels optimizes the reconfiguration time with a factor up to 4x than that of the network of wormhole routers without virtual channels.

1. Introduction

Many applications, mapped on SRAM-based FPGAs (Field Programmable Gate Arrays), such as signal processing, including image and video, software defined radio (SDR) [1], and electronic measurement applications are increasingly using Dynamic Partial Reconfiguration (DPR) feature. Moreover, partially reconfigurable (PR) devices save chip area by programming only the necessary physical resources in each operation phase. Accordingly, area and power are saved by programming only the desired block, which allows for static leakage reduction.

The prime factor to check the feasibility of using DPR techniques, such as ICAP and JTAG, is the available lead time, which is the latency between the configuration and the initiation of a PR, and denoted by: reconfiguration time (RT). Consequently, more researchers aim to optimize the RT of DPR that is related and limited to the frame size of SRAM-based FPGA layouts [1].

Due to the continuous scaling of CMOS devices, manufacturers are increasing the number of functions implemented on a single chip. Therefore, the concept of System-on-Chip has been introduced, which consists of processing elements (PEs) and storage elements (SEs) connected by a complex communication architecture.

Within the last few years, communication among these PEs is destined to become a vital factor in the design of large-scale systems. As the focus is to increase the number of PEs in parallel in order to maximize the capability of modern designs, thus the processing power has increased and data-intensive applications have emerged. Consequently, several challenges of the communication among these PEs, when configured on FPGAs, have become significant and require innovative solutions. Therefore, a prominent concept for communication known as Network-on-Chip (NoC) has been adapted for FPGAs to handle these PEs communication challenges.

To investigate this NoC concept, a state-of-art tool denoted by NoC-DPR is developed [2], which is a cycle-accurate simulator for NoCs that support DPR. This tool is used to simulate the performance of NoC-based FPGA. In NoC-DPR, a NoC simulator namely: NoCTweak [3] and a SystemC Library called ReChannel [4], which is a DPR simulation library, are integrated. All PEs of NoC are reconfigured dynamically to

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adopt a new application at run-time.

This paper is organized as follows. Section 2 provides an overview of previous related research efforts in DPR simulation and NoC simulation. In Section 3, the NoC-DPR simulator architecture is presented. Section 4 investigates the NoC-DPR performance compared to NoCtweak simulator. In Section 5, The DPR experiment is analyzed along with the results. Section 6 illustrates the case study of the embedded application using NoC-DPR simulator. Design insights and recommendations to implement DPR for NoC-based FPGA are stated in Section 7. Finally, Section 8 concludes the paper and presents the future work.

2. Related work

Since the first generation of Xilinx FPGAs that support DPR, Virtex-II at early 2007 [1], the design for DPR was a slight complex task due to the lack of supporting tools, and the requirement of full understanding of the FPGAs architecture. Therefore, FPGA designers use DPR simulators at early design stages as a proof of concept, and to reduce the time to market. Several approaches [5–7] have been proposed to model dynamically reconfigurable systems at system-level using SystemC, which is C++-based description language used at higher abstraction levels to develop complex systems. In Ref. [8], the OSSS + R framework and design methodology for automatic modeling, synthesis, and simulation of partial run-time reconfiguration systems are presented. This framework has the underlying philosophy to treat dynamic reconfiguration separately from a system's functional specification; the tool then automatically generates the necessary reconfiguration controls.

The modeling is performed using object-oriented techniques, and with avoiding the limitations of SystemC at modeling dynamic reconfiguration. Such as ReConLib library [8]. As the main challenge when modeling dynamic designs using SystemC is the inability of performing changes to the system's module topology during simulation. This leads to difficulties in the modeling of reconfigurable systems using hardware description language (HDL) without modifications. The ReChannel library [4] is an extension to SystemC, not a modification to SystemC kernel as conducted in previous projects, which overcomes SystemC modeling limitation without actually changing the underlying simulation kernel.

On the other hand, several NoC simulators have been developed recently. Some of the simulators are developed in C++ such as Booksim by Jiang et al. [9] that allows simulating NoC within a broad range of topologies, buffer sizes, and routing algorithms. Currently, Booksim 2.0 features more detailed modeling of the router micro-architecture, models inter-router channel delay and provides support for additional traffic models. Others simulators are developed in SystemC such as NIRGAM by Jain et al. [10], a NoC simulator for mesh and torus typologies. Also, SystemC-based Noxim by Catania [11] that is a wireless Networks-on-Chip (WiNoCs) simulator to address the scalability limitations of conventional multi-hop NoC architectures. Simulation parameters such as routing algorithms, buffer depths, and configurable traffic patterns are allowed to be varied in the Noxim algorithm. Currently, Noxim supports virtual channels routers and reports only the network performance. Similarly, Palesi et al. developed a simulator in SystemC [12], it supports wormhole routers over synthetic traffic patterns. In addition, NoCTweak has been written in SystemC by Anh et Bevan [3] which supports multiple router types (wormhole, wormhole with virtual-channels) over both synthetic traffic and embedded application patterns as portrayed in Fig. 1.

Others approaches attempt to use NoC as a backbone in FPGAs system to overcome communication challenges, such as Ehliar and Liu [13] that proposes an open source FPGA based NoC architecture with low area overhead, high throughput, and low latency compared to the general NoC performance. Another architecture with similar features is ReNoC developed by Stensgaard and Sparse [14]. The latter proposed architecture allows NoC components to be reconfigured; thus, the topology is customized for the application that is currently running on a generalized System-on-Chip (SoC) platform.

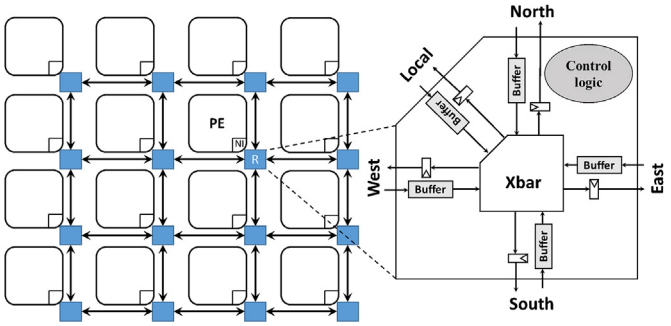

Fig. 1. Architecture of NoCTweak simulator.

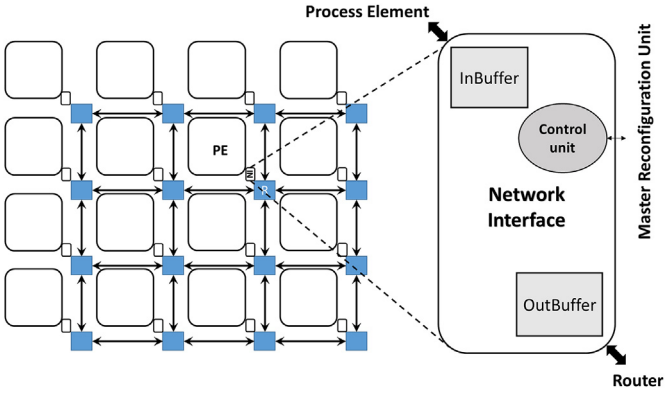

Fig. 2. Architecture of NoC-DPR simulator.

3. NoC-DPR simulator architecture

NoC-DPR simulator is a command line based tool that consist of a 2-D mesh network of routers, simulated by NoCTweak [3], as illustrated in Fig. 2. Each node consists of a Processor Element (PE), Network Interface (NI), and an associated router. Each router connects with four nearest neighboring routers forming a 2-D mesh network. Using ReChannel [4] library, each PE is dynamically reconfigured by a special type of data packet, generated from certain node (master node 0, 0). Data packets are injected into the network through its router. Packets are routed to their destinations in the network of routers by the selected routing algorithm.

When merging DPR simulation library with NoC simulator, the main consideration that must be taken, is all NoC's modules should be well-defined through a clear hierarchy at SystemC. Consequently, a separate NI is implemented with NoC-DPR simulator as displayed in Fig. 2. Accordingly, DPR is performed on the PE, and NI supports the flow control over receiving and sending data during the DPR operation. However, network's latency and throughput values have changed due to this modification, and are discussed in Section 4.

3.1. NoCTweak simulator

NoCTweak has been developed using SystemC which allows accurate and fast modeling of concurrent hardware modules at the cycle-level accuracy [3]. The simulator is an open-source 2-D mesh NoC simulator for early exploration of on-chip networks performance. NoCTweak is composed of a hierarchy of modules; processor (core), a network interface (NI), and an associated router that implements different functions of the network and the simulation environment as portrayed in Fig. 1. Each of these modules has a well-defined interface that facili-