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Analog perceptron circuit with DAC-based multiplier

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ABSTRACT

This paper presents a perceptron circuit which can be implemented into a sensor analog front-end consistent with neural network-based machine learning. We introduce a DAC-based multiplier in the perceptron circuit, where the DAC is used as a programmable resistor. Compared with a traditional transconductor-based multiplier, the precision of our multiplier is formulated only by the digital codes, and it has a wide input range and a good temperature dependency. The simulation result demonstrates the DAC-based multiplier amplifies smoothly analog signal by the digital codes. Furthermore, we extend our perceptron model so as to deal with time series inputs and show a promising result by simulation. As one of an important future works, focusing on periodic signal inputs, we discuss a general architecture of perceptron circuit inspired by Fourier series.

1. Introduction

In recent years, a machine learning has remarkably developed, and many cases of its social implementation have been reported. A neural network is one of fundamental architectures for the machine learning, and the VLSI (very large scale integrated circuit) implementation has been researched traditionally [1]. Recent trends of machine learning implementation are configuration on FPGAs (field programmable gate arrays) and acceleration by GPUs (graphics processing unit) [2,3].

On the other hand, a wireless sensor network is widely used to collect data in various area such as factories, farms, and cities. An advanced sensor node has a multi-input to compensate a sensing information by employing different sensor signals. For example [7], introduces an 8-channel EEG(Electroencephalogram)/electrode-tissue impedance acquisition system, where nine active electrodes and one back-end analog signal processor work being closely correlated. In Ref. [8], a pressure sensor and a microphone are combined to visualize the blood pressure measurement.

In the compensation and combination of input signals, it is known that a machine learning technique is useful. Hence, a sensor node is requested to incorporate an architecture for neural network computing. Unlike GPU or FPGA-based neural network architectures, however, a sensor node must be low power and with a small hardware even sacrificing a large computation.

Therefore, we attempt to embed a learning circuit mechanism into an analog front-end of a sensor node. This paper focuses on a perceptron which is an essential function of neural networks. Aiming a small embedding, we realize it by analog circuits introducing a DAC(digital-analog-converter)-based multiplier in the perceptron circuit. The DAC-based multiplier is to amplify an analog input signal by a preset digital code. Compared with a traditional analog multiplier of transconductor-based, the precision of our multiplier is formulated only by the digital codes, and it has a wide input range and a good temperature dependency. The simulation result demonstrates a perceptron circuit with the DAC-based multiplier smoothly combines multiple analog signals amplifying by the digital codes.

Furthermore, we introduce a phase shifter to our perceptron model to divide an input signal into time series inputs with the same phase delay. The simulation results convince us that the extended perceptron circuit is applicable to prediction algorithms such as a recurrent neural network and chaos pass filter.

In addition, as one of future works, we discuss a general architecture of a perceptron circuit to represent any signal in the output based on Fourier series.

The rest of the paper is organized as follows. Section 2 describes a perceptron circuit used in neural network systems. Section 3 introduces a DAC-based multiplier and describes the simulation results. Section 4 describes an idea and examples of time series input with phase shifters. In Section 5, we discuss a general architecture of our perceptron circuit focusing on periodic signals. Section 6 summarizes this work.

2. Perceptron circuit

As described in Ref. [1], a perceptron is an essential function used in neural network systems. A typical model of the perceptron is illustrated in Fig. 1. The inputs are $f_1(t)$ …, $f_n(t)$, each of which is multiplied by a

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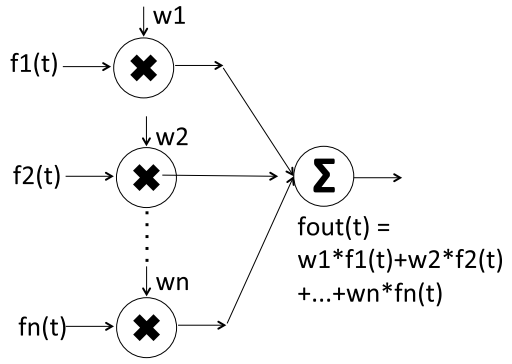

Fig. 1. A typical perceptron function.

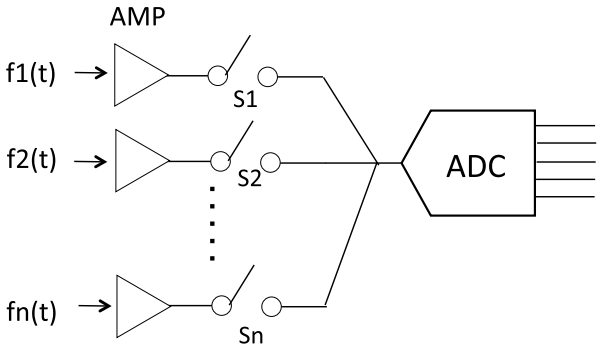

Fig. 2. An example of analog front-end with time division multiplexed input.

weight w_1, …, w_n, and all weighted inputs are summed at the output.

In general, realizing this perceptron function in an analog front-end of a sensor node, time division multiplexed input is used. Here, as shown in Fig. 2, each input of $f_1(t)$ …, $f_n(t)$ is controlled by switches S_1 …, S_n exclusively, and a selected input is transmitted to the ADC. Plus, in an application of biological sensor systems, an input signal is so tiny, an input analog buffer is placed at each input. However, a VLSI implementation yields a variation of amplitudes among the input analog buffers due to a process-induced variation, and it degrades the precision of sensing values.

To avoid degrading the precision of analog values, an analog multipliers and adder are used as shown in Fig. 3. In this figure, Vin1 and Vin2 are amplified by the weight signals, w1 and w2, respectively. The input is connected to the variable resistor which is realized by a transconductor of PMOS or NMOS transistor [6]. The weight value is

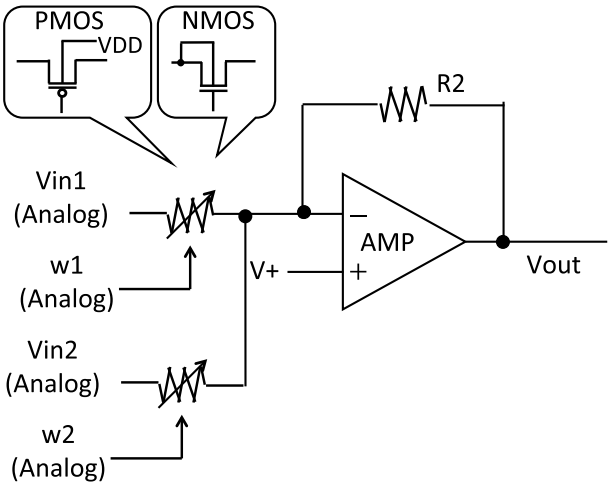

Fig. 3. Analog multiplier and adder for perceptron.

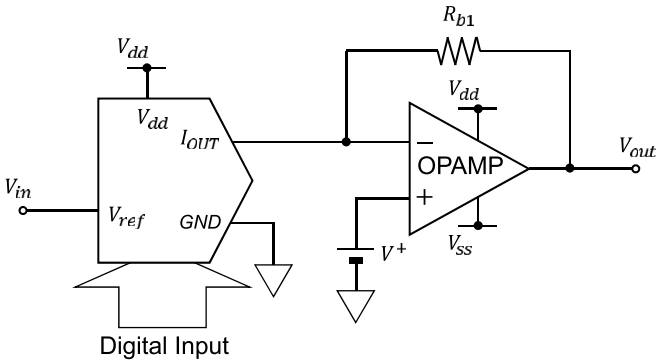

Fig. 4. A programmable gain amplifier pattern (1).

determined by a ratio of the variable resistor and R2. However, this implementation also has a defect in the temperature dependency and the input range, which are described below.

3. DAC-based multiplier

3.1. DAC-based programmable gain amplifiers

We adopt two types of programmable gain amplifiers introduced in Ref. [4] to realize a multiplier overcoming defects described above. The schematics of the programmable gain amplifiers are illustrated in Figs. 4 and 5 (called pattern (1) and (2), respectively). Both patterns basically configure the negative feedback of the opamp, but he resistance in the feedback is replaced by the DAC.

In detail, the DAC is inserted at the input of the negative feedback circuit in pattern (1), while it is at the loop of the feedback in pattern (2). Changing of the DAC output current looks as if the resistance value were to change.

We design these patterns and verify the function by the simulation. All circuits are designed with a model of 0.6 μm/5 V manufacturing process. The V_{tn} and V_{tp} of NMOS and PMOS are 0.7 V and 0.9 V, respectively. Plus, β_n and β_p are 1.0×10^{-4} A/V^2, 0.4×10^{-4} A/V^2. A typical two-stage opamp used in this paper is shown in Fig. 6, and the specification of the opamp is shown in Table 1. As well, the schematic of the DAC is illustrated in Fig. 7.

In the simulation, we observe the changing of the output amplitude for pattern (1) and (2) when changing the DAC input codes from zero to the fullscale, and the results are shown in Figs. 8 and 9, respectively. In Fig. 8, we can observe the output amplified by $N \cdot R_{b1}$. As well, the

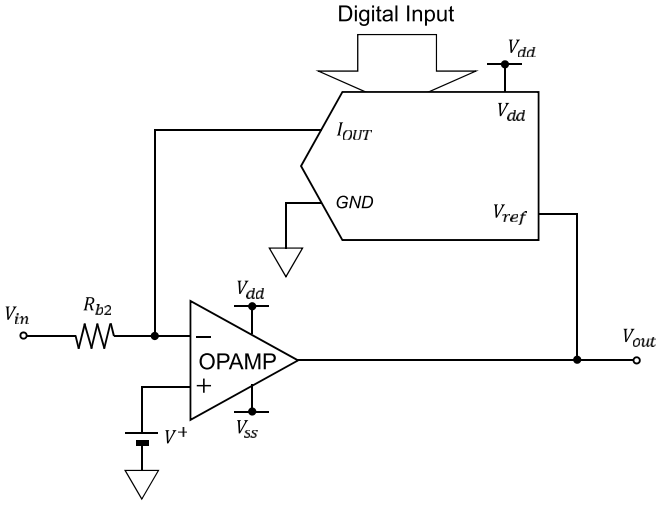

Fig. 5. A programmable gain amplifier pattern (2).