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Second-order compensation BGR with low TC and high performance for space applications

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ABSTRACT

This paper presents a new Bandgap Voltage Reference (BGR) design, with second order curvature compensation, for space applications. The work focuses on the design of the different analog building blocks which integrate the BGR. The proposed design, also, includes the complete implementation of trimming networks, which is a post-fabrication technique that strongly improves the performance in all the special conditions that characterize the target environment. The circuit was designed in a 150 nm Silicon-on-Insulator CMOS technology node, using radiation-hardened components. Simulation results with typical models show a performance of 0.758 ppm/°C for temperature coefficient over a military temperature range, with a 1.25 V output voltage, which competes with the actual state-of-the-art solutions.

1. Introduction

Bandgap reference (BGR) circuits are widely used in the context of both analog and digital circuitry and are considered of utmost importance in nowadays electronic systems. This block provides a specific and steady DC voltage, which ultimately tends to be completely independent of external variations with degrading impact in the performance of a circuit, i.e., fabrication changes due to process variations, supply voltage trimming, and, also, surrounding temperature variations.

During the 21st century, the field of electronics evolved tremendously by adding new devices, new techniques, and topologies, which allow an excellent performance and reliability on reference circuits. Traditionally, the BGR provides an output voltage close to the silicon bandgap voltage, which is often around 1.22 V. The original reference circuits use Bipolar Junction Transistor (BJT), due to their parasitic characteristics which help to achieve the desired voltage. The typical types of BJT used on these circuits are the vertical BJTs.

The increasing interest in compact equipment has led to reduce both the size of transistors and the supply voltages. Due to this, a new stream of BGR circuits focuses on MOSFET-only components, letting the use of these reference blocks in sub-1 V applications with lower power consumption. However, the clear majority of the proposed architectures are liable to suffer from severe drawbacks in space environments. The space radiation (Total Ionizing Dose - TID) affects the sensitivity of the components causing variations in the output. This is one of the most challenging problems caused by complex space radiation, i.e., the effects in electronic devices caused by accumulated fluxes of high energy charged particles X-rays and gammas, resulting in a deviation of the devices' behavior from the nominal one. Moreover, abrupt temperature changes and aging often accelerate components degradation. Overall, the complexity that represents the design and optimization of a complete space system, which must have a satisfactory performance over the complete operating range, requires a robust design with elevated stability margins. Additionally, the reliability is often in line with somehow elevated power consumption, in the order of hundreds of microwatts and the usage of widely tested topologies [3,6].

This paper addresses the utmost need for high reliability demanded in space industry together with high performance and low power consumption, by proposing the design of a BGR with curvature compensation with enhanced robustness and voltage precision. In this work, a temperature coefficient (TC) of 0.758 ppm/°C, over a military temperature range of −55 to 125 °C was achieved, considering a 3.3 V supply source and a reference output voltage of 1.25 V. The implementation was carried out in SOI CMOS 150 nm process technology with radiation-hardened components as enclosed layout transistors (ELT) and using a technique to reduce the radiation impact [6,7]. The presented work is an extension of [1]. When compared to the state-of-the-art, the proposed circuit has the following advantages:

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- Reduced impact of radiation, using a radiation-hardened SOI ASIC technology (ATMX150RHA), improving the resistance of the circuit to TID, Single Event Effects (SEE) and Single Event Latch-up (SEL);
- The optimal sizing for each block is implemented, meaning a smaller area and less expensive circuit, with the best performance;
- A simple adjustment of the output voltage featured due to the implemented trimming;
- Low TC consistency within a military range temperature corner conditions;
- The possibility to use as Intellectual Property (IP) for similar projects;

This paper is structured as follows: Section 2 describes the fundamentals of BGR, as well as, the presented topology; Section 3 presents the design of the sub-blocks; Section 4 shows the results; and in Section 5, the conclusions are drawn.

2. Background &state-of-the-art

The voltage reference block is a circuit that generates a very precise output voltage. Ideally, this circuit is not affected by the input voltage, load current, temperature, time or any other undesired disturbance. This circuit is often confused with a voltage regulator, however even when both circuits are quite similar, the accuracy between these systems distinguishes one from the other, i.e., the voltage reference is a circuit with far higher precision in its output signal, with a reduced noise, a long-term stability and lower power consumption [2].

A voltage reference performance can be evaluated in terms of its reliability and accuracy. The system performance in steady-state, suffer an influence from the regulations in the line, load, and mismatches in the components. Hence, in the transient state it is influenced mostly by the factors below:

- Temperature Coefficient
- Line Regulation
- Power Supply Rejection Ratio (PSRR)
- Output Voltage Noise

2.1. Operating function

The operation principle of the circuit is based on the generation of two components, the Proportional-to-Absolute Temperature (PTAT) and the Complementary-to-Absolute Temperature (CTAT). This is represented in (1), where the reference output is the weighted sum of these two components. The m and n elements are weighting parameters for the equation.

$$V_{REF}(T) = m{*}V_{PTAT}(T) + n{*}V_{CTAT}(T) \quad (1)$$

2.2. Second order compensation

The high order compensation is often known as curvature compensation [2]. Theoretically, the adjustment to obtain a near-zero temperature coefficient voltage is based on the proper scale of CTAT and PTAT voltages, whose changes are never exactly proportional to temperature. The extension of a voltage with second-order TC to the appropriate temperature region will increase the reference voltage in the selected temperature region, and thus archive a low TC reference voltage over a wider temperature range.

The second order temperature dependent voltage is expressed in (2), where S(T-Tnom)^2 is the second order temperature dependent voltage, in which s is a constant form the Taylor series. Fig. 1, shows a topological diagram of a second order compensation for the temperature in a BGR circuit.

$$V_{REF}(T) = m{*}V_{CTAT}(T) + n{*}V_{PTAT}(T) + s(T - T_{nom})^2 \quad (2)$$

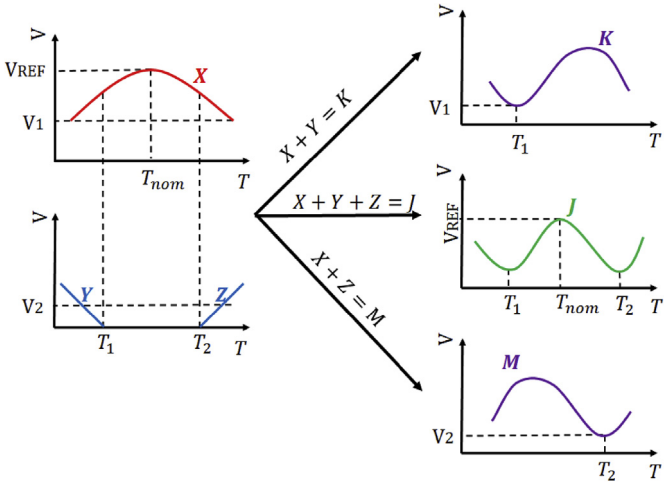

Fig. 1. Representation of a second order compensation of BGR.

Table 1
Specifications of the BGR.

Voltage Reference [V]	Supply Voltage [V]	Current Consumption [mA]	TC [ppm/°C]	PSRR [dB]
1.25	3.3	< 1	< 10	> 60

2.3. Specifications

The specifications for this project are presented in Table 1, where the BGR must be stable and with 7 bits to program the trimming section. An important request for this implementation is the feature that helps to avoid the radiation effects, i.e., the usage of a specific process technology and a minimum current per branch (mcpb), as throughout explained in Refs. [6,7].

2.4. State-of-the-art & topology selection

A wide assortment of topologies for second order compensation has been published in the last decade [4,7,11–24]. These architectures are implemented with several stages and background techniques; however, every topology follows a similar principle for the compensation.

A comparison between these circuit topologies by year is presented in Table 2. Thus, choosing a suitable architecture to implement took several considerations, making difficult to select a topology suitable for a set of specific characteristics. Based on the complexity of the topologies, and from the design point of view it is more practical to implement the different stages of the circuit as simple blocks.

The proposed circuit is an adaptation of the work proposed in Ref. [3], which allows the achievement of the space industry specifications, as demonstrated in Ref. [4] for a different technology node. Thus, the selection of the architecture took into account the simplicity of implementation and the easiness to adapt different topologies in each block. The BGR published in Ref. [4] is a predecessor of the work presented in this paper, which is a detailed extension of the one presented in Ref. [1], pointing out the different topologies in some sub-blocks such as Bias, Power Down and Trimming section, technology and techniques.

The chosen topology is older when compared with recent topologies [4,7,11–24], however, this architecture, does not only allow adaptive modifications in the different blocks but also proves to have the needed performance indexes, in a recent implementation as demonstrated in Ref. [4].

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