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Architectural exploration of perpendicular Nano Magnetic Logic based circuits

U. Garlando, F. Riente*, G. Turvani, A. Ferrara, G. Santoro, M. Vacca, M. Graziano

Dipartimento di Elettronica e Telecomunicazioni, Politecnico di Torino, Corso Castelfidardo 39, 10129, Torino, Italy

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ABSTRACT

Perpendicular NanoMagnet Logic (pNML) can be considered one of the most interesting emerging technology since it has unique features that cannot be naturally implemented with standard transistor technologies. Each device can act both as a memory and a logic circuit. Because of its intrinsic properties, this technology makes it possible to easily design 3D circuits. In this paper, we propose several complex architectures by exploiting the 3D integrability of the pNML technology. The presented circuits belong to different categories, covering both combinational and sequential circuits. Memory elements and logic circuits have been designed and simulated taking into account the technology constraints. As an absolute novelty, the first Finite State Machine based on pNML is also introduced.

1. Introduction

The scaling of CMOS performance and sizes is reaching its physical limit [1]. Moore's law for clock frequency began to fail in the past years. Now, also dimension scaling doesn't follow that rule anymore. The main problems of nowadays technology are the physical dimension and power density. Photolithography is becoming more and more expensive to enable the scaling of transistor dimensions. Furthermore, the increasing transistor density inside an integrated circuit leads to different problems due to power consumption. To overcome some of these issues new structures have been developed. Transistors with more than one classic gate, like Fin-Fet, are the only way to continue shrinking devices.

On the other hand, researchers are focusing on completely different technologies able to overcome CMOS limitations. A possible alternative can be found in field-coupled devices. Identical bi-stable cells are used to store a single bit of information [2]. The behavior of the circuit is defined by the interaction among neighboring cells. Among the field-coupled technologies, Nano Magnet Logic (NML) [3] and its out-of-plane implementation, the perpendicular NML (pNML) [4], is the most promising. In this technology, bi-stable single-domain nanomagnets are used to store binary information. One of the main advantages of pNML is that current technological fabrication processes can be used to fabricate these kind of devices [5], which can be integrated with standard CMOS [6]. Furthermore, nanomagnets are capable of storing non-volatile logic information [7] with a reduced power consumption. Indeed, no current flows through the elements during computation. Another benefit brought in by pNML is the intrinsic capability of fabricate 3D circuits [8,9]. Magnets can be placed on adjacent planes creating a new way of designing digital circuits. Nevertheless, some drawbacks are still present in pNML technology, for example, operating frequency is an order of magnitude lower than CMOS.

The working principle of field-coupled technologies breaks down the design rules adopted for CMOS technology. The continuous interaction among adjacent elements leads to information constantly moving through the circuit. These characteristics create the need for a complete redesign of the well know basic elements adopted in digital architectures.

In this paper, we present the design of several kinds of digital circuits implemented in pNML technology. To the best of our knowledge, no such circuits were ever presented in literature since now. The circuits showed in this work represent the basic components normally adopted within a complex digital architecture. Memory elements, programmable logic and arithmetic circuits are described in the following sections. Furthermore, a Finite State Machine (FSM) based on pNML technology is introduced. The circuits have been designed using MagCAD [10], a tool that we have created to easily design and analyze pNML circuits. The correctness of the designs has been proved through simulations.

The paper is organized as follows: the technological background is provided in section 2. Section 3 gives an introduction of the design framework and the adopted methodology. Here, the set of chosen circuits vary from combinational to sequential circuits. In section 4, we propose the design of pNML Random Access Memory, a 32-bit Ripple

* Corresponding author.
E-mail address: fabrizio.riente@polito.it (F. Riente).

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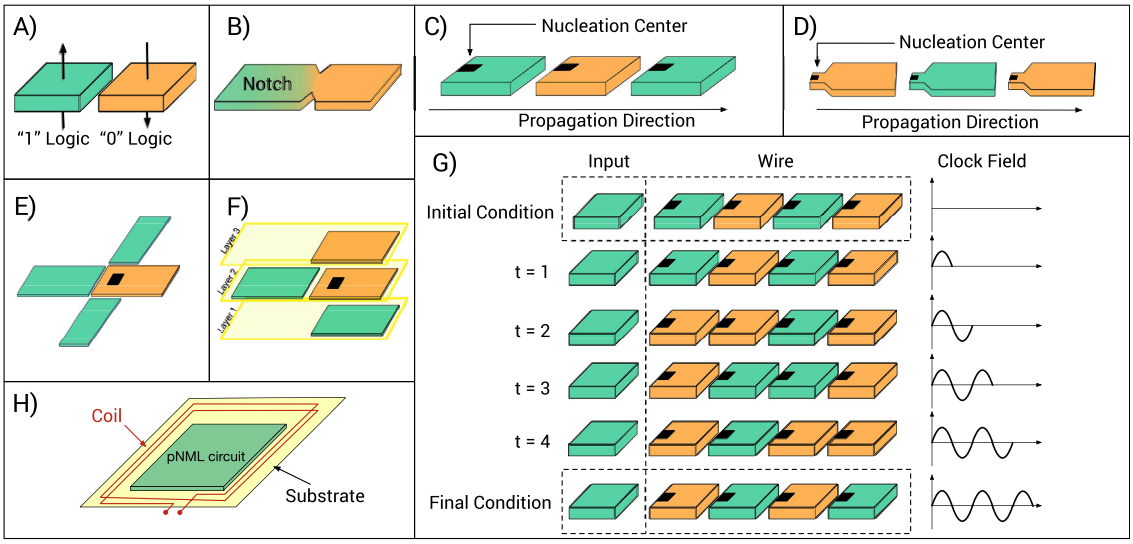

Fig. 1. NML: (A) magnetic binary representation; (B) Notch; (C) (D) pNML wire; (E) (F) pNML majority voter; (G) pNML clock mechanism. (H) Clock coil representation.

Carry Adder, a Programmable Logic Array and an FSM. The proposed architectures have been simulated to verify their behavior. We extracted circuits' performance such as area, clock frequency and latency. Furthermore, these elements can be combined together to build complex circuits exploiting the Logic in Memory (LIM) paradigm [7,11].

2. Background

In pNML technology, single domain nanomagnets with perpendicular magnetic anisotropy (PMA) are used to represent the binary information. The magnetization vector encodes the logic '1' and '0' [3,12] as depicted in Fig. 1A. In pNML technology, information propagation is accomplished differently from CMOS; here, each magnet is a non-volatile memory element. The PMA is obtained with a multi-layer stack of Co/Pt. The number of layers and their thickness define the magnetic properties of the device [13]. By placing magnets one near the other, it is possible to obtain a wire (Fig. 1(C)). Two neighboring magnets try to reach the minimum energy configuration; thus, opposite magnetization direction. However, the magnetic interaction among neighboring magnets is not enough to enable the magnetization reversal. Two additional elements are introduced to guarantee a correct information propagation: the clock mechanism [14] and the artificial nucleation center (ANC) [15]. The former is needed to help the magnetization reversal when the superposition of the clock field and the coupling field, coming from neighboring cells, are present. The latter, instead, defines the information propagation direction.

An example of the clock mechanism is depicted in Fig. 1(G). In pNML technology, the clock field is a sinusoidal magnetic field, perpendicular to the magnets plane, applied to the whole circuit. In order to generate this magnetic field, coils are placed beneath the magnets. Fig. 1(H) shows how the coil can be 3D integrated in pNML technology. The clocking apparatus corresponds to the "power supply" in CMOS circuits [16]. To understand its behavior, consider that a new input is placed near a pNML wire in stable conditions (Fig. 1(G)). The input magnet and the first element of the wire have the same magnetization direction. The anti-ferromagnetic interaction tries to force an opposite value on the first magnet, but the coupling field is not enough. When the clock field has the same direction of the "desired" value, the superposition of the two forces leads to the magnetization reversal. This situation is verified at t = 1 in the example. At time t = 2 the first two elements of the wire have the same magnetization, and the clock field has inverted its direction. The same condition as before are verified and also the second magnet can switch to the new value. The process is repeated for the successive time instants until the input is transferred to the output. The minimum energy configuration is preserved even if the clock field continues oscillating.

The problem of information direction is not solved by the clock field. The process described before works only if it is possible to ensure that the magnet on the right will be the switching one. The ANC is used to force this behavior. By changing the magnetic properties on a specific spot of each magnet, it is possible to define a region more sensitive to magnetic field changes. The ANC is the area of the magnet where the nucleation of the domain wall takes place. In this area the magnetic field needed to force a new value is less with respect to the rest of the magnet. Considering Fig. 1(C), the darker part of each element identifies the ANCs. In this example, the left magnet is able to influence the one to its right, while the contrary is not possible. Thus, the only allowed propagation direction is from left to right. Normally the ANCs are obtained through a Ga^{+} Focused Ion Beam (FIB) irradiation. The FIB changes the magnetic properties of the irradiated part, lowering the magnetic anisotropy. A different way for creating the ANC has been presented in Ref. [17]: a modification in the magnet geometry and the fabrication process leads to the same result as FIB irradiation. An example can be seen in Fig. 1(D). In pNML technology, the main logic gate is the Majority Voter (MV), Fig. 1(E). By placing three different magnets near an ANC it is possible to define a MV. The output of this logic gate is the opposite of the majority of the inputs, due to the anti-ferromagnetic interaction. Note that a MV with a fixed '0' input behaves as an AND gate, while a '1' defines an OR gate. Furthermore, 3D circuits are intrinsically enabled by the technology [6]. Fig. 1(F) shows a compact version of the MV. In that case, two inputs lay on different planes with respect to the gate. Considering that MV can work with an odd number of inputs [18], it is easy to create very compact layouts.

pNML technology provides also a synchronization element. Fig. 1(B) shows a notch [19]. This element, thanks to its particular shape, pins the incoming information [5,7]. An additional magnetic field, parallel to the magnet plane, is needed to lower the energy barrier restoring the information propagation in the notch. This in-plane field is called the de-pinning clock. The de-pinning clock is generated by a wire passing under the notch.

Digital circuits can be divided into different categories. The main distinction is between memory and logic. Random Access Memory (RAM) is an example of circuits belonging to the first category. RAMs are composed of a matrix of memory cells: rows define a word of data, while columns are the available addresses. In a RAM, values are stored at a specific address. Data can be retrieved by simply giving the correct address and enabling the read