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3-Path SiGe BiCMOS power amplifier on thinned substrate for IoT applications☆

Sefa Özbek [a,*], Golzar Alavi [b], Johannes Digel [a], Markus Grözing [a], Joachim N. Burghartz [b,c], Manfred Berroth [a]

[a] Institute of Electrical and Optical Communications Engineering (INT), University of Stuttgart, Stuttgart, Germany
[b] Institute of Nano- and Microelectronic Systems (INES), University of Stuttgart, Stuttgart, Germany
[c] IMS CHIPS, Stuttgart, Germany

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ABSTRACT

This paper reports a transformer-based integrated class-A Differential Power Amplifier (DPA) for the Internet of Things (IoT) applications. The proposed 5–6 GHz fully integrated differential PA is fabricated in a cost-effective 95 GHz-*f*max, 0.25 μm SiGe BiCMOS technology (IHP process SGB25V). The amplifier utilizes a thin Si chip with a thickness of 45 μm in order to be embedded into flexible electronic foil systems. Several key RF performance parameters of the DPA with different substrate thicknesses are evaluated at the wafer level. The measurement results indicate that the DPA shows no significant S-parameters degradation due to the thickness differences. The measured gain center frequency is shifted about 300 MHz towards higher frequencies after thinning because of the image mirror currents within the conducting material at the backside of the chip. The DPA achieves 10.65 dB and 9.7 dB small-signal gain at 5.5 GHz before and after thinning, respectively. The PA delivers an output power of +9 dBm before and +8.1 dBm after thinning process at $P_{in} = -1.3$ dBm. The simulated 1 dB compression point occurs at +10.76 dBm output power with a PAE of 15%.

1. Introduction

Radio Frequency IDentification (RFID) system architecture has been advanced for more than half a century, hence their applications with recent developments are numerous. Silicon technologies are constantly being improved, and multiple electronic devices can now be integrated onto a single chip by semiconductor industries. Moreover, the achievements in RFID technology recently inspire emerging technologies to combine with the Internet [1]. Such a network of physical devices is called as the Internet of Things (IoT). IoT basically allows objects such as Radio-Frequency Identification (RFID) tags, NFC, mobile networks, wireless network sensors (WNS) and WLANs, etc. to sense or interact with each other [2]. Therefore several challenges in wireless data communication systems such as communication speed, reliability, and energy efficiency are also valid for IoT applications to provide seamless connectivity [3].

The growing demand for the modern wireless communication systems leads to an extra complexity in the system design. However, several specific requirements are difficult to meet in their combination due to the technological constraints:

- long-range and broadband wireless data communication
- environment-agnostic and high efficient wireless data communication
- small and mechanically flexible devices

Among these criteria, the mechanically flexible device is the most demanding requirement due to its sophisticated thinning process. In addition, it brings another constraint, such as stringent cooling requirement, to design and causes performance degradation.

In order to be embedded into flexible foil systems, the device must be reasonably small, mechanically flexible and therefore thin. Due to thin Si substrate, the vertical thermal resistance to the package is lower compared to their bulk Si chips, while the lateral thermal resistance is expected to be higher due to the small cross-sectional area [4,5]. In addition, the maximum surface temperature in a flexible polyimide substrate is higher because of a poor thermal conductivity of the polyimide substrate. Furthermore, owing to the feasibility of future systems-in-foil, there should exist as few external components as possible, which includes an inductor, transformer, and switches [6].

Fig. 1 illustrates the block diagram of the proposed flexible module

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* Corresponding author.
E-mail address: sefa.oezbek@int.uni-stuttgart.de (S. Özbek).

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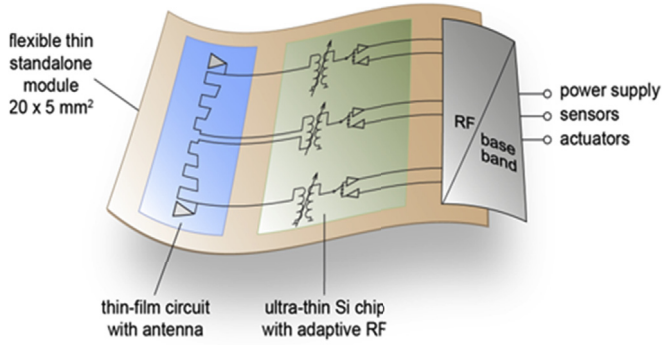

Fig. 1. Block diagram of the proposed flexible module containing flexible chip and antenna on a polyimide substrate.

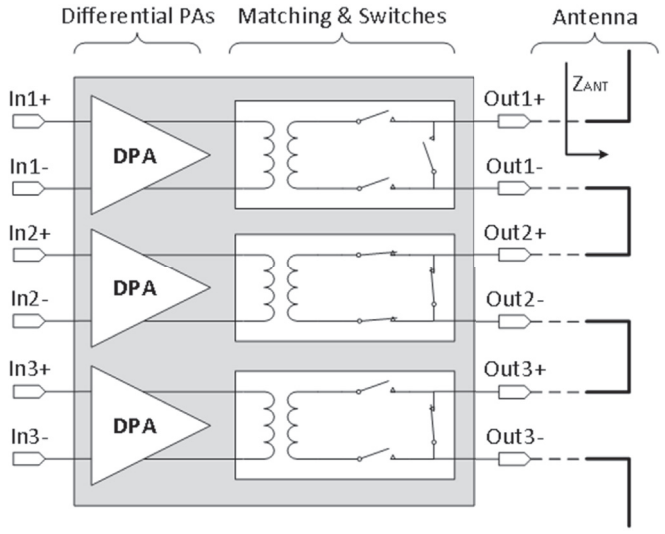

Fig. 2. Block diagram of SiGe based power amplifier array.

containing flexible chip and antenna on a common substrate. The proposed flexible chip consists of a Transmit/Received (T/R) switch, PA, and a low noise amplifier (LNA). In order to keep power consumption within limits and to provide high communication data-rates, the technology used in the proposed project must be very fast and low-parasitic. This can be achieved far easier with silicon technology than with organic thin-film electronics. In terms of integration density, stability, robustness and circuit performance, organic thin-film electronics lags behind the silicon technology. To overcome these challenges, a low-cost and high speed 0.25 μm SiGe BiCMOS technology is used for circuit design.

The main reason for the high temperature in overall transceiver (TRX) systems is the significant self-heating of the power amplifier (PA) because of the great amount of power dissipation and the low thermal conductivity of the polyimide substrate. Therefore, in this work, a fully integrated class-A mode differential PA for 5–6 GHz frequency band has been studied at the die level before and after thinning. The required frequency bands of 5–6 GHz are less congested compared to the popular frequency band of 2.45 GHz and offer more bandwidth per channel. The aim of the DPA is to be able to deliver +10 dBm output power within the required frequency band. Various RF parameters are measured on a vacuum chuck, which may relate to the substrate thickness and residual stress in the silicon [7].

This paper is an expanded version of the 13th Conference on PRIME, Giardini Naxos, Italy, June 12–15, 2017 [8]. The simplified block diagram of three identical differential PAs is shown in Fig. 2. The outputs of DPAs are matched for maximum output power by using a transformer. The secondary part of the transformer is connected to fully integrated RF switches that are intended to connect the PA array to a multi-feed antenna. The antenna-transmitter-array is able to adapt to different antenna environments such as high- and low-permittivity dielectric media (textile fabric, human skin and other parts of the body such as blood or body), by using different feed access points of the antenna. To provide optimum isolation and insertion loss, the topology of series/shunt switch configuration is used. In addition, the shunt switches may also be used to change the phase of the multi-feed antenna. The RF switch parasitics are also considered as a part of matching circuits to improve the linearity of PAs.

This paper is structured as follows. The specification of the power amplifier is defined in Section 2. In Section 3, the proposed broadband transmitter design including I/O matching, differential PA, transformer, and switches is presented. Section 4 describes the thin chip fabrication shortly. Section 5 focus on the thermal characterization of thin silicon chips. The post layout and experimental results of the design before and after thinning process are given in Section 6. Finally, we present our conclusions in Section 7.

2. Power amplifier specification

The RF power amplifier boosts the output power level of the transmitter and delivers the power to the antenna. The power rating is the most significant specification of the power amplifier since it impacts directly the communication capacity. In order to design the PA, the first step is to calculate the saturated power (P_{SAT}). The power level of the DPA can be estimated by summing up the required average output power at the antenna and the overall loss between DPA and antenna, i.e., the loss of I/O Matching and T/R switch. The presented DPA is designed to evaluate the effect of the thinning process on the RF performance of circuits at 5–6 GHz frequency band, therefore its specifications are not considered as strict as a PA design for IEEE 802.11ac standard [9]. P_{SAT} is defined as:

$$P_{\mathrm{SAT,PA}}(\mathrm{dBm}) = P_{\mathrm{antenna}}(\mathrm{dBm}) + Loss_{\mathrm{switch}}(\mathrm{dB}) \tag{1}$$

As mentioned in Section I, the required output power from the system is about +10 dBm within the frequency band of 5–6 GHz. Assuming the inevitable overall loss mainly caused by the switch insertion loss is 3 dB, the targeted output power of the DPA core is +13 dBm.

In this study, a “class A” mode amplifier design is performed due to linearity concerns. In class A mode, the bias point of amplifier defines full conduction angle (2π) with the small input signal, thus the output waveform is only distorted owing to inherent distortion of the device. Although class A operation offers the highest linearity and stability, it suffers from poor efficiency as compared with other classes of operations such as AB, B and C [10,11]. The low efficiency is the reason for the large power consumption at the transistors.

In this design, DPAs are supplied with 1.5 V using npn-HBT with 2.4 V the maximum collector to emitter voltage. The maximum differential output power is given as

$$P_{\mathrm{out,Diff}} = \frac{V_{\mathrm{pk,SE}}^2}{R_{\mathrm{opt,SE}}} \tag{2}$$

where $R_{\mathrm{opt,SE}}$ is half of the differential load seen at the collector of the transistor. Thus, the optimum load impedance can be calculated by assuming the peak output voltage swing of 1 V after the saturation voltage and the required output power of 13 dBm. According to the calculation, a differential load impedance of 100 Ω is required to avoid efficiency degradation due to the non-optimum load impedance. Accordingly, the total DC current consumption is equal to 60 mA.

The efficiency of class A mode amplifier can be expressed as:

$$\eta = \frac{P_{\mathrm{RF}}}{P_{\mathrm{DC}}} = \frac{i_c \times V_{\mathrm{pk,SE}}}{2} \times \frac{1}{I_{\mathrm{DC}} \times V_{\mathrm{DC}}} \tag{3}$$