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1GigaRad TID impact on 28 nm HEP analog circuits

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ABSTRACT

An in-depth analysis of modern technologies could represent the base for the success of the High Luminosity Large Hadron Collider experiments. The requirement is a new reliable electronics in 1Grad-TID environments. For the purpose, single devices in TSMC 28 nm bulk CMOS technology have been realized and studied. Preliminary experimental results demonstrate nMOS structures more resistant than pMOS. Nevertheless, the considerable leakage current increment is not negligible because it could affect analog circuits as the pixel readout channel hereby presented. In the particular case, the high radiation level induces a gain reduction and a slowdown of the time response.

1. Introduction

Reliability and radiation hardness are two main aspects to be evaluated with particular attention in the High Energy Physics world. The CERN Large Hadron Collider (LHC) will undergo a major upgrade after 2022 (High Luminosity LHC, HL-LHC). According to [1,2], the luminosity will reach a peak of $5\text{–}7 \times 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$ (around 10 times higher than current value) and will produce collisions at a rate of about 5×10^9/s. The expected Total Ionizing Dose (TID) peak will reach 1GRad in the innermost layer of the pixel detector in 10 years of operations and the electronics will have to be capable to tolerate so high TID levels. The new detector systems will have countless potential that could be restricted by radiation-affected Integrated Circuits (ICs). The upgrade of the silicon pixel sensors for the HL-LHC experiments requires the development of new readout integrated circuits due to unprecedented radiation, very high hit rates and increased pixel granularity. High performance electronics in 1 Grad environment is a challenge and the choice of a suitable technology is fundamental.

Classical technology scaling down, based on gate-oxide thickness reduction, has been performed up to 90 nm, until the gate-oxide leakage was no longer negligible. Then, the high-k dielectric introduction [3] has allowed to manage this issue and to carry on further size reduction. As described in details in Refs. [4,5], the TID effects in nanometer technologies must be investigated case-by-case and they depend on the specific high-k material. For example, ultra-thin Reoxidized Nitrided Oxides (RNO) could show an extremely good radiation hardness unlike Hafnium Dielectrics [5].

TID effects are classified as long-term ones because they induce long-term changes at transistor parameter level and analog circuit performance. Instead, the wide range of the possible Single Event Effects (SEEs) depend on single ionizing particles affecting mainly digital and memory parts with unpredictable bits loss, spurious signals or devices destruction. Although the advanced CMOS technologies may show a major total dose tolerance, the SEE sensitivity should be carefully evaluated in scaled technology nodes. CMOS TID hardness scaling trend can be found in Ref. [6].

For the HL-LHC upgrade, both ATLAS and CMS experiments have chosen the 65 nm bulk CMOS process for the production of the pixel readout chip. Future HEP projects, where pixel granularity and functionality will have even more stringent requirements, force to look at new technologies. These nowadays offer options in terms of minimum gate size (65 nm, 45 nm, 32 nm, 28 nm, or below), technology features (CMOS-bulk, CMOS-FinFET, CMOS-SOI, etc …) and technology access and cost. CMOS-SOI is not an option for such TID level, given the poor

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tolerance to radiation of the thick buried oxide. In the ScalTech28 experiment, we will investigate the TSMC 28 nm bulk CMOS node for future new pixel design, in order to take advantage of higher digital circuit density, higher speed and, hopefully, increased rad-hard performance. This choice is a good compromise between circuit performances, design complexity and production costs.

The study of the technology performances with respect to TID is therefore a mandatory step before the electronic design. In particular, investigation on single structures would help to select the most suitable devices for each application, considering that the geometry influences the TID-induced damages. A trade-off between area occupancy and radiation hardness is essential and must be evaluated in the design phase. In addition, the results coming from the single devices studies must be taken into account in the critical points of analog circuits. The large variation of pMOSFET parameters (i.e. voltage threshold or transconductance) implies to prefer nMOSFET architecture, especially when some specifications should change in a limited range.

In Section 2 of this paper, some important details on 28 nm single devices behavior are given. Two similar facilities located at the Department of Physics and Astronomy of the University of Padova and at CERN, were used to investigate nMOSFET and pMOSFET parameters variation in presence of high TID levels (up to 1 Grad). In particular, from the study done in Padova, it results that the nMOSFETs demonstrate an increase of leakage current above the expectations (increment of 2–3 orders of magnitude) and a reduction of the threshold voltage limited to maximum 30 mV. In the same conditions, a drop of saturation current and up to few hundreds of mV of threshold voltage shift result for pMOSFETs. These radiation-induced effects could compromise the analog performance of ICs. Similar features appeared from CERN analysis as published in Refs. [7,8], validating most of the conclusions hereby presented.

Section 3 of this paper is addressed to an activity carried out in parallel, regarding the implementation of a typical HEP pixel read-out system. Testing the latter in the same conditions, a global overview on this 28 nm technology has been obtained and could be very helpful to consider and mitigate (if possible) TID radiation effects during electronic ICs design. Preliminary experimental results have been reported showing leakage induced gain reduction and system slowdown. At the end of the paper, conclusions will be drawn.

2. 28 nm Total Ionizing Dose studies

2.1. Overview

Single transistor test structures have been irradiated up to a Total Ionizing Dose (TID) of 1 Grad (SiO_2) to investigate the potentiality of this technology with respect to radiation hardness for applications in instrumentation electronics for particle physics.

2.2. Test structures and measurement setup

The irradiated test structures consist of two sets of 10 single core-transistors (one set with n-channel, the other p-channel), with standard V_{thr}, different geometries and diode-based ESD protection; transistors of each set share the same substrate, source and n-well contacts, while drain and gate contacts are accessible for each individual device. The different geometries available (W is the width, L the length of the gate channel) are:

- W = 3 μm and L = 1 μm, 30 nm;
- W = 1 μm and L = 30 nm, 60 nm, 90 nm;
- L = 1 μm and W = 100 nm, 200 nm, 400 nm;
- L = 30 nm and W = 100 nm, 300 nm

The TID tests have been carried out at the X-ray facility installed at the Physics and Astronomy Department of the University of Padova [1,9]. A photo of the naked chip is reported in Fig. 1. It was mounted on a semi-automatic 4-inch wafer probe station within the X-ray irradiation cabinet and contacted by a custom probe card. The probe card features 32 probe tips (two columns of 16). A Keithley 707 switching matrix connects the four Single-Measuring-Units (SMUs) of the semiconductor device analyzer (HP4156) and the voltage supply to specific probe tips. In this way, the selected set of structures could be properly biased during irradiation and measurements. Given the limitation in the number of connections available in the switching matrix, only one set of transistors could be biased and irradiated at a time. This meant that we performed the irradiation study on different dies for nMOSFETs and pMOSFETs. Only one sample was studied for each type of transistor.

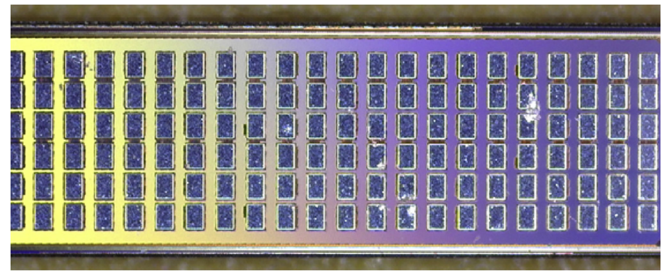

Fig. 1. Photo of single devices matrix.

The chip was placed as close as possible to the tube exit in order to maximize the dose rate, which could be set at 8 Mrad/h (SiO_2). During irradiations, the devices were kept with both drain and gate biased, while source and bulk were shorted to ground [10]. These are not the typical worst-case bias conditions used for MOSFETs in TID studies, but they are the bias values the largest damage in the 65 nm technology node. For nMOSFETs the conditions were $V_{DS} = V_{GS} = 1.1$ V; for pMOSFET $V_{DS} = V_{GS} = -1.1$ V. The value 1.1 V is 10% more than the technology nominal supply voltage and has been chosen since it maximizes the damage +10% is the maximum tolerable value guaranteed by the foundry.

Irradiations were performed at room temperature up to 1 Grad, in steps. Measurements were taken before irradiation and after each dose step. The whole setup was remotely controlled, so that the sequence of irradiation and measurements could be performed automatically. No annealing was performed afterwards, given limitations to the available setup.

2.3. MOSFET irradiations

2.3.1. Leakage current

The main TID effect on linear-layout nMOSFETs is the positive charge trapped in Shallow Tranch Isolation (STI) oxides, which opens a lateral conductive path where current can flow between source and drain. This current, flowing in the lateral parasitic transistor, appears as an increase of the leakage current in the main transistor.

In Fig. 2, the evolution of the leakage current is shown, as a function of TID, for all the transistors tested. Leakage current increases of 2–3 orders of magnitude for all the transistors, regardless of the geometry. Saturation current (Fig. 3) does not display any appreciable degradation, so that the I_{on}/I_{off} ratio is always greater than 10^4.

Therefore the degradation of leakage current should not affect the overall device functionality, even though it would cause a large increase of power consumption in very complex circuits.

2.3.2. Threshold voltage

Fig. 4 shows the V_{th} evolution with respect to TID for the whole set of transistors. V_{th} value was extracted with the maximum transconductance method in the linear region [11]. It can be noted that, with the exception of the narrowest transistors, the V_{th} decrease is limited to <30 mV (and it is within the device-to-device variability); for transistors with a small W,

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