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Scalable lumped models of integrated transformers for galvanically isolated power transfer systems

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ABSTRACT

This work presents a review of integrated transformers for galvanic isolation with particular focus on their modelling in power transfer systems. A comparison between transformer-coupled oscillator topologies is carried out, highlighting the main differences in the realization of the isolation transformers. Lumped geometrically scalable modelling of the most adopted isolation transformer topologies are presented and compared. Transformer models have been validated by means of electromagnetic simulations in a wide range of geometrical parameters, achieving absolute errors lower than 12% for inductance, *Q*-factor peak, self-resonance frequency, and magnetic coupling factor.

1. Introduction

Galvanic isolation of several kilovolts is usually required to electrically separate different functional interfaces in several applications (e.g., gate drivers, industrial, automotive and medical equipment etc.), thus guaranteeing both safety and reliability in harsh environments. Traditionally, galvanic isolation was implemented by means of optocouplers and/or discrete transformers. Such expensive and bulky solutions are going to be replaced by miniaturized galvanic isolators based on electromagnetic (EM) coupling i.e., transformers [1,2], and capacitors [3]. Indeed, these new galvanic isolators can directly be integrated on-chip or fabricated with post-processing techniques. While capacitors are mainly exploited in data-communication isolators, transformers can be used to transfer both power and data across isolating interfaces. As shown in Fig. 1(a), a typical transformer-based dc-dc converter is essentially made up of three blocks, a VHF power oscillator, an isolation transformer, and a rectifier. Firstly, the oscillator implements a dc-ac conversion of the supply power, P_{IN}, then the transformer delivers the ac power to the rectifier across the galvanic barrier. Finally, the rectifier performs an ac-dc conversion and delivers the dc power, P_{OUT}, to the load on the isolated side. The state-of-the-art of such isolated dc-dc converters is represented by highly integrated solutions able to transfer up to 1 W with power efficiencies up to 30% across a 5-kV galvanic isolation barrier [4–7]. Differently from commercially available products, they integrate both the oscillator and the transformer within the same die, which is connected by bonding wires to a second chip housing the rectifier, as shown in Fig. 1(b). In these systems, the galvanic isolation is performed by a thick-oxide layer between the transformer primary and secondary windings, built with on-top metal layers [8]. The most critical block in fully integrated converters is the isolation transformer, which greatly contributes to the power efficiency and power density performance. Moreover, the interaction between dc-ac converter (i.e., oscillator and transformer) and ac-dc converter (i.e., rectifier) is highly non-linear. Therefore, an accurate modelling of the isolation transformer is required to enable an iterative co-design procedure between blocks, which is mandatory to maximize the overall dc-dc conversion performance. Unfortunately, a reliable modelling of on-chip transformers is not trivial. Indeed, it is a difficult task to obtain high accuracy by using lumped networks whose components are defined by physical expressions based on both technology back-end and layout geometries. On the contrary, model accuracy is often achieved by means of distributed high-order networks with numerical fittings, thus completely losing any link with the physical devices. Such models are not useful in the design phase, where it is required to explore different transformer geometries in a co-design approach between active and passive blocks of the converter.

This work reviews the design guidelines for integrated transformers in galvanically isolated dc-dc converters. Scalable models are proposed for three isolation transformer configurations [9] (i.e., stacked,

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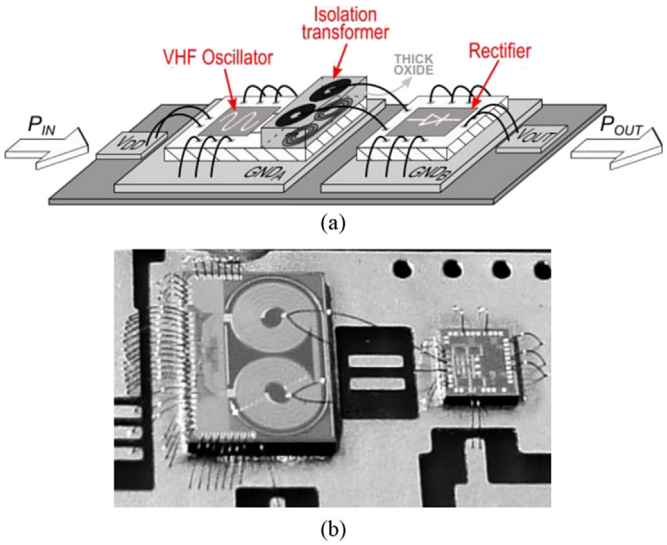

Fig. 1. Fully integrated dc-dc converter with on-chip isolation transformer (a) Block-diagram and (b) typical silicon implementation [4].

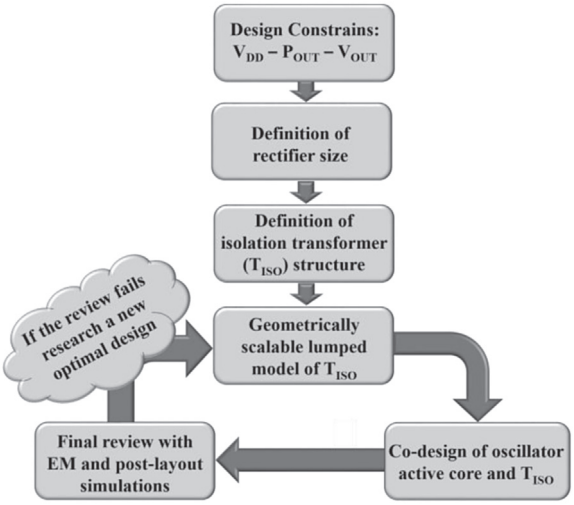

Fig. 2. Design procedure for galvanically isolated power transfer systems.

three-winding interleaved and three-winding tapped), typically used in power oscillator topologies [4–7]. The paper is organized as follows. Section 2 describes typical transformer-based power oscillator topologies for galvanically isolated dc-dc converters, along with corresponding isolation transformer structures. Section 3 is focused on scalable modelling of isolation transformers. Finally, main conclusions are drawn in Section 4.

2. Galvanically isolated power transfer systems

Typically, isolated dc-dc converters adopt transformer-loaded power oscillators, since they represent a straightforward solution for galvanic isolation, while performing efficient dc-ac conversion. Isolation is guaranteed by a proper dielectric layer between the stacked windings of the transformer. On the other hand, the rectifier usually exploits traditional full-bridge topologies that achieves high power efficiency without increasing system complexity. If available, Schottky diodes are used for a better rectifier efficiency. The design of the fully integrated dc-dc converter poses several challenges since it is characterized by non-linear interactions between each building block, thus requiring system optimization to obtain the maximum efficiency. The overall dc-dc converter efficiency, η, is the product of the efficiency of each building block operating into the whole system, as in the following equation

$$\eta = \eta_{CORE} \times \eta_{TR} \times \eta_{RECT} \quad (1)$$

where η_{CORE} is the efficiency of the active oscillator core, η_{TR} is the efficiency of the isolation transformer, and η_{RECT} is the efficiency of the rectifier. Indeed, the bottleneck of the power flow from the supply power, P_{IN}, to the dc power delivered to the load, P_{OUT}, is the isolation

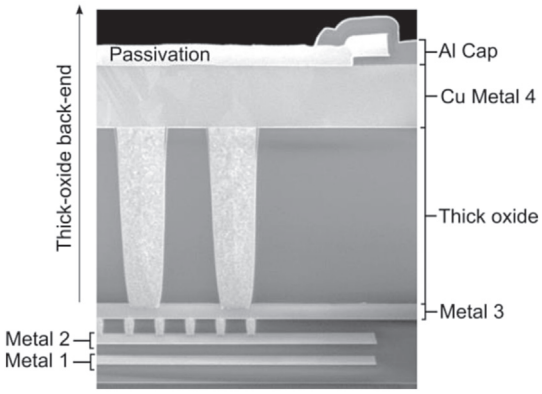

Fig. 3. SEM cross-section of the process metal stack with thick-oxide option.

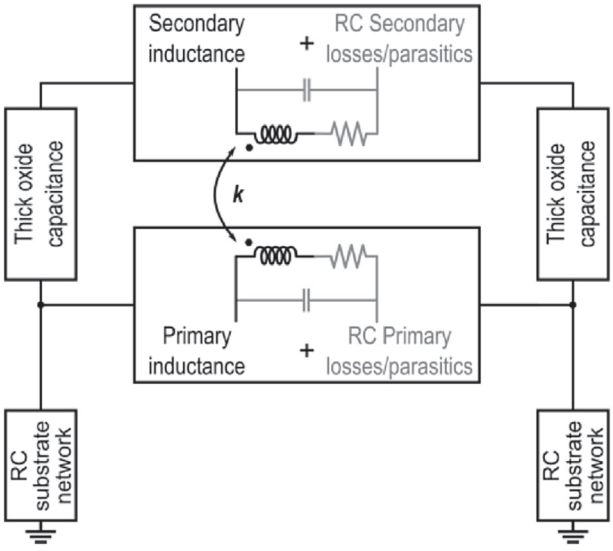

Fig. 4. Simplified scheme of an integrated isolation transformer model.

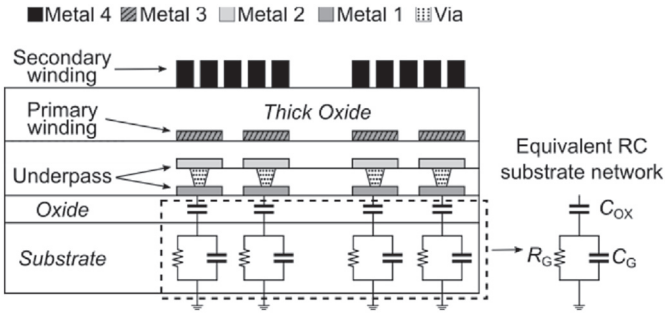

Fig. 5. Technology cross-section with equivalent networks for the substrate.