Integration, the VLSI Journal xxx (2017) 1–11

Contents lists available at ScienceDirect

Integration, the VLSI Journal

journal homepage: www.elsevier.com/locate/vlsi

Enhanced systematic design of a voltage controlled oscillator using a two-step optimization methodology

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ARTICLE INFO

Keywords:
Radiofrequency
Process parameter variations
Multi-objective optimization
Voltage controlled oscillator
Integrated inductors modeling

ABSTRACT

In this paper a design strategy based on bottom-up design methodologies is used in order to systematically design a voltage controlled oscillator. The methodology uses two computer-aided design tools: AIDA, a multi-objective multi-constraint circuit optimization tool, and SIDe-O, a tool that characterizes and optimizes integrated inductors with high accuracy (around 1% when compared to electromagnetic simulations). By using such tools, the difficult trade-offs inherent to radio-frequency circuits can be explored efficiently and accurately. Furthermore, with the capability that AIDA has at considering process parameter variations during the optimization, the resulting methodology is able to obtain truly robust circuit designs.

1. Introduction

First-pass fabrication success has always been a constantly-pursued, yet difficult-to-attain, aspiration for the integrated circuit (IC) designer. By ensuring a first-pass success, the designer avoids costly re-design cycles and post-fabrication tuning work [1], which considerably decreases the efficiency of the design process. Radiofrequency (RF) circuits are among the most difficult ones to ensure first-pass fabrication success due to their complexity and high operation frequencies. In the last few years, there have been tremendous advances in RF technologies, pushing forward the state-of-the-art with higher operation frequencies and improved circuit performances, enabling technologies such as 5G [2]. Therefore, the design of such RF circuits is nowadays very defiant and challenging, pushing the RF designer to its limit.

Nowadays, designers use an established manual design procedure that relies on their own experience. In traditional and manual design approaches, the designer follows an iterative procedure to size each active and passive device in the circuit, as in Ref. [3]. Additionally, in this type of design procedures, analytical equations that describe the basic circuit behaviour are commonly used. This set of equations is specifically derived for each circuit topology, limiting their general use. Moreover, this kind of design approach also presents the following drawbacks. Firstly, the analytical expressions used to model the circuit performances and the impact of the device physics are usually too simplified (to be of any practical use), and, hence, inaccurate. Secondly, passive devices such as, integrated inductors, are very difficult to model and most analytical models do not present a reliable characterization. Thirdly, the device extreme performances (e.g., process corners) are usually not taken into account on a first design iteration, and are only considered after a functional nominal design is reached.

Due to the abovementioned issues, it is clear why these manual design strategies usually need to be refined by a considerable number of design iterations. Therefore, in order to avoid these iterations and speed up the design process, new systematic approaches are required to reduce the development cycles of RF circuits.

In this sense, evolutionary computation techniques have been applied to the design of RF circuits in recent years [4–7]. The use of optimization-based methodologies tries to overcome the traditional knowledge-based methodologies by using optimization algorithms that automatically explore the design space in order to find optimal designs. However, most optimization-based methodologies still use inaccurate inductor models, such as analytical models (e.g., the π-model in Ref. [8]), and most of them do not consider process parameter variations during optimization, drastically reducing the possibility of achieving robust designs.

In order to accurately model highly sensitive passive components,

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https://doi.org/10.1016/j.vlsi.2018.02.005
Received 29 September 2017; Received in revised form 8 February 2018; Accepted 10 February 2018
Available online xxxx

such as integrated inductors, designers aiming for high performance designs typically rely on electromagnetic (EM) simulators. Some approaches integrate these accurate simulations into optimization-based methodologies [9]. In these approaches, the optimization loop becomes computationally intensive due to the EM simulations, and, therefore, the efficiency of the design process dramatically deteriorates. Alternatively, relying on inductor libraries provided by the foundries [6], overcomes the efficiency problem. However, these libraries offer limited inductor choices and, therefore, reduce the possibility of finding an optimal inductor for a given application. Alternately, lumped-element models (e.g., the π-model [8]) relating performance parameters with the inductor geometric parameters can provide a wide range of inductor choices on a reasonably efficient evaluation time-cost. Unfortunately, these models are not entirely accurate, especially at high frequencies [10].

In this work, an optimization-based approach is adopted to systematically design a voltage-controlled oscillator (VCO) [11], where the passive component problem is tackled by using a state-of-the-art surrogate modeling technique that provides less than 1% error when compared with EM simulations. Furthermore, by considering extreme corner performances for each candidate solution during the optimization process, robust designs are provided.

The remainder of this paper goes as follows. Section 2 describes the basics of VCO design and their design parameters, as well as the most relevant performances, illustrating the problems faced in manual-design strategies. Section 3 presents an automated corner-aware design approach, and, Section 4 presents experimental results. Finally, conclusions are drawn in Section V.

2. Voltage controlled oscillator design insights

The VCO is a circuit whose oscillation frequency is controlled by an input voltage. From the several VCO topologies available, in this work a cross-coupled double-differential VCO is considered, as depicted in Fig. 1. In order to have an oscillation, a negative resistance must be generated to compensate the parasitic resistance of the VCO tank (formed by the capacitor, C, and inductance, L). In the circuit presented in Fig. 1, both the PMOS and NMOS transistors are used to provide sufficient negative resistance to make the oscillator operate uninterruptedly. This LC-VCO topology shows good phase noise performance as well as low power consumption [3]. From the available voltage and current biasing techniques, the current one is selected in this work due to its lower power consumption [3].

In this specific topology, there are 16 initial design variables: the p-type and n-type MOS transistors' dimensions (w_{n1}, w_{p1}, l_{n1} and l_{p1}), the geometric parameters of the integrated inductor (number of turns n, inner diameter D_{in}, turn width w and spacing between turns s), the varactor dimensions (w_{var} and l_{var}), the capacitor value (C), the dimensions of the transistors used to bias the circuit (w_d, w_{dd}, l_d and l_{dd}), and also, the bias current (I_{Bp}).

Typically, the most important performance parameters in VCO designs are the oscillation frequency (f_{osc}), the phase noise (PN), the frequency tuning range, the power consumption (P_{DC}), the output voltage swing (V_{OUT}), and also, the circuit area, which is extremely important as it directly relates to the manufacturing cost in IC technologies. Based on the desired performances, a design strategy must be considered.

In order for a VCO to oscillate properly, the designer has to guarantee that the negative resistance (given by the MOS transistors) is higher than the resistance imposed by the tank (mainly by the inductor). Therefore, an established rule-of-thumb is that the following condition, the so-called start-up condition, is reached:

$$g_{active} \geq \alpha \times g_{tank} \quad (1)$$

where g_{active} and g_{tank} are the transconductance of the MOS transistors and the tank loss, respectively, and α is a constant value, often between 2 and 4. The oscillation frequency f_{osc} is given by:

$$\frac{1}{\sqrt{LC_{max}}} \geq f_{osc} \geq \frac{1}{\sqrt{LC_{min}}} \quad (2)$$

where L is the inductance and C_{min} and C_{max} are the tank minimum and maximum capacitance, which vary due to the varactors.

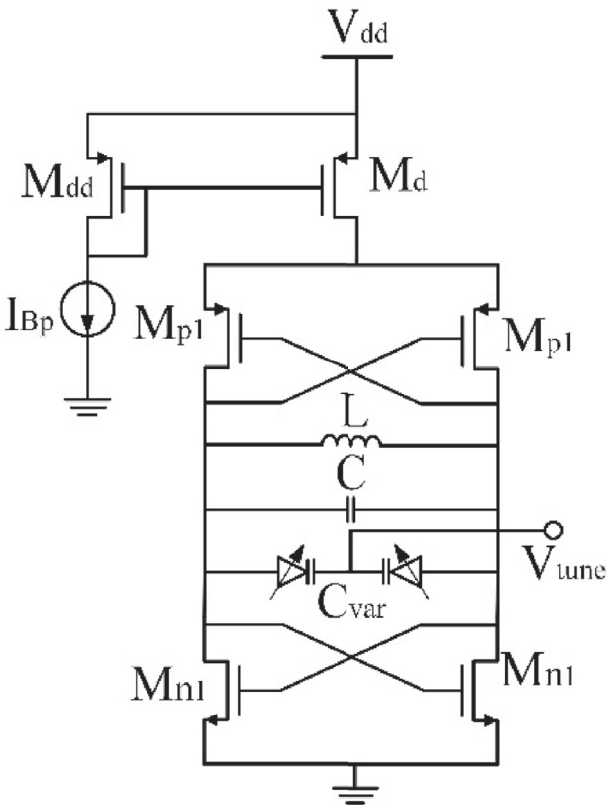

Fig. 1. Cross-coupled double differential VCO topology.

Apart from f_{osc}, which does not need special design techniques, other performances that must be considered demand special design techniques, such as the minimization of phase noise or power consumption [3]. These strategies are not trivial and require some specific design procedure and a great deal of tweaking that comes of the expert knowledge from the designer. One of the most common design strategies that usually fulfils both, phase noise and power specifications, can be summarized as follows. The designer must find the minimum inductance that satisfies both the start-up condition and the output power. Then, the maximum bias current allowed by the design specifications is chosen. This will ensure the maximization of the output swing and the minimization of the phase noise. Furthermore, the tank capacitance also introduces a trade-off in the design, where large capacitances improve the phase noise but reduce the tuning range [3,12].

In summary, the design of such VCOs is not trivial and, frequently, re-design iterations are needed in order to achieve the desired specifications. Moreover, in these traditional design methodologies, adopted by the majority of RF designers, the corner simulation is only performed after the sizing task is completed. Therefore, this introduces even more discrepancies, which leads to even more re-design iterations between circuit sizing and final tape-out, due to the fact that the impact of the devices' extreme corner performances is in most times harsh. Therefore, in order to solve the re-design issues, an optimization algorithm that searches for optimal designs can be considered. Also, in order to obtain more robust designs, a corner analysis can be included during the optimization using a corner-aware approach.