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Full Length Article

Analysis and implementation of impedance source based Switched Capacitor Multi-Level Inverter

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ABSTRACT

In recent years, a numerous Multi-Level Inverter (MLI) topologies are proposed with reduced number of switches and control complexity. An Impedance source based MLI structure with ability of additional boost is proposed in this work. The proposed topology requires one source, one impedance network and reduced number of switches when compared to recently reported inverter literature. Due to Self-voltage Balancing circuit (SBC), the fixed boost of 1.5 times the input and equal voltage across all the capacitors are achieved. An additional boost is obtained by placing impedance network between input source and SBC. The proposed Inverter is compared with existing topologies with respect to a number of sources, number of impedance networks, control switches, voltage balancing and boost capability. A simple level shifted based sinusoidal pulse width modulation technique is adopted for generating gate pulses. Further theoretical analysis and computer aided simulation results are validated with the experimental results.

1. Introduction

Novel MLI topology has significant advancement in the field of power electronics, because of numerous advantages over conventional inverters. The conventional two level inverters are facing difficulty in meeting present scenario. The most popular conventional MLI structures are: Diode Clamped MLI (DCMLI), Flying Capacitor MLI (FCMLI) and Cascaded H Bridge MLI (CHMLI) [1–3]. In DCMLI, (n-1) capacitors are used as potential dividers, the voltage unbalancing across these capacitors is a serious concern. Additionally, it requires (n-1)(n-2) clamping diodes. For FCMLI, (n-1)(n-2)/2 bulky capacitors are required. In CHMLI, separate sources are required for each H Bridge and each bridge produces three levels. These H Bridges are connected in series for generating the required number of levels in output voltage where n is number of levels in output waveform.

A numerous MLI topologies are proposed to address the drawbacks of conventional MLI's. In recent years the focus is made on:

Increasing the number of levels in output with asymmetrical voltage sources as reported in [4–6]. These inverters require more than one source with different voltage magnitudes. To obtain different voltages, different turn's ratio transformers are used. The asymmetrical MLI requires DC sources with different magnitudes and switches of different rating.

A few topologies are proposed by reducing the number of switches [4,7–9] and sources [10–12]. To reduce the number of input sources, series connected capacitors are used as a potential dividers. To achieve balanced voltage across all DC-link capacitors, a separate feedback circuit is used [13,14]. Inverter circuit will become complex due to this approach.

With the conventional or transformer based MLI's [15–18], in case of any shoot through or miss gating, entire circuit will get damaged. The cost and losses increases due to transformer present in the circuit.

In aforementioned topologies, the maximum available voltage is limited by the input or DC link voltage. In applications like: Photovoltaic system, Electrical vehicles, Dynamic voltage restorer, etc. requires both boost and buck operations [19]. To meet this normally DC-DC converter or Z Source Inverter (ZSI) is used. If a DC-DC converter or Z Source network is integrated with MLI, then separate DC-DC converter or Z network is required across each source [20]. This leads to increased size and cost.

This paper proposes a modified MLI topology, which addresses the drawbacks of conventional inverters and recently reported

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inverters. The proposed system consists of single DC source with the single impedance network to enable boost operation. A bank of series connected capacitor is used as potential dividers without any feedback circuit. To overcome the limitations with asymmetrical voltage, simple self-voltage balancing technique [21] is used for maintaining equal voltage across DC-link capacitors.

The rest of the paper is organized as follows. In Section 2, working of proposed topology along with the modes of operation is explained. Section 3 deals with extended proposed structure. The analysis of the entire inverter circuit is discussed in Section 4. Detailed comparison is presented in Section 5. Simulation and experimental results are shown in Section 6 followed by conclusion in Section 7.

2. Proposed topology

The proposed topology shown in Fig. 1 consists of two parts.

Part 1 is Self-voltage Balancing Circuit (SBC), composed of capacitors C_1 – C_5, out of which C_1 & C_2 are the DC bus capacitors and C_3 – C_5 are flying capacitors and clamping switches S_{C1} to S_{C6}. Part 2 is 7-level inverter topology with level generating switches S_5 – S_7 and H Bridge switches S_1 – S_4.

The working of part 1 is shown in Fig. 2. The switches used in SBC are divided into two groups. Group 1 consists of S_{C1}, S_{C3} and S_{C5} and Group 2 consists of S_{C2}, S_{C4} and S_{C6}. SBC operates in two modes. In mode I, Group 1 switches are gated and in mode II, Group 2 switches are gated. The gate pulses should develop such

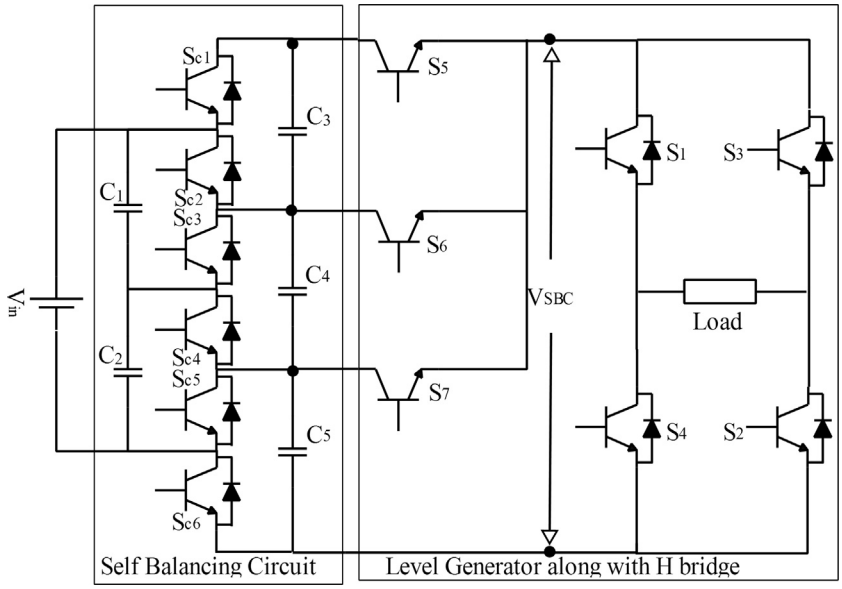

Fig. 1. Proposed Topology.

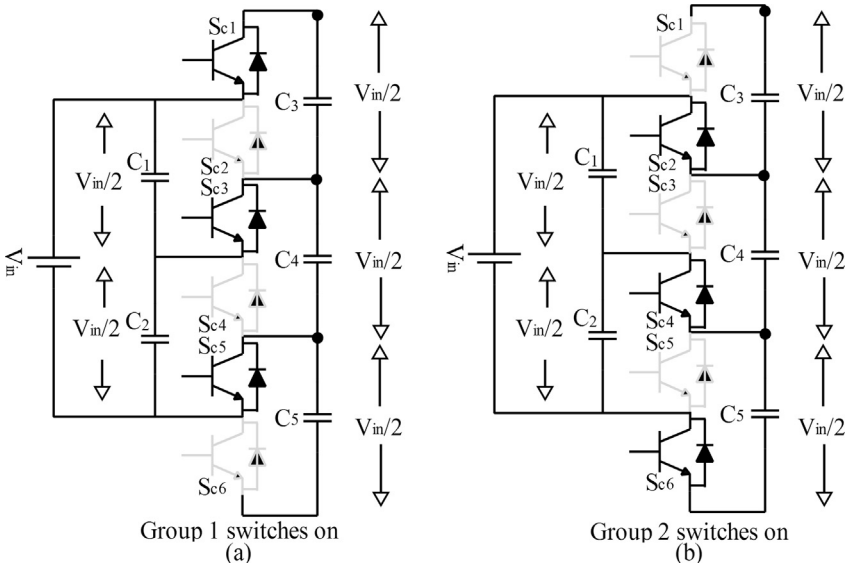

Fig. 2. Mode of operations of SBC. (a) Mode 1 and (b) Mode 2.