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A tunnel FET compact model including non-idealities with verilog implementation

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ABSTRACT

We present a compact model for Tunnel Field Effect Transistors (TFET), that captures several non-idealities such as the Trap Assisted Tunneling (TAT) originating from interface traps (D_{it}), along with Verilog-A implementation. We show that the TAT, together with band edge non-abruptness known as the Urbach tail, sets the lower limit of the sub-threshold swing and the leakage current at a given temperature. Presence of charged trap states also contributes to reduced gate efficiency. We show that we can decouple the contribution of each of these processes and extract the intrinsic sub-threshold swing from a given experimental data. We derive closed form expressions of channel potential, electric field and effective tunnel energy window to accurately capture the essential device physics of TFETs. We test the model against recently published experimental data, and simulate simple TFET circuits using the Verilog-A model. The compact model provides a framework for TFET technology projections with improved device metrics such as better electrostatic design, reduced TAT, material with better transport properties etc.

1. Introduction

Tunnel Field Effect Transistors are promising candidates for low power logic applications [1]. They have the potential to reduce energy dissipation by relying on Band To Band Tunneling (BTBT) for carrier injection, achieve steep turn-ON and thus reduce the supply voltage. Under ideal conditions, device simulations consistently reported switching at sub-thermal rates [2–8]. Even though the output current from TFET may be low, a sub-thermal sub-threshold swing has the potential to drastically reduce power dissipation and therefore it is attractive for low power applications. Many compact models have been developed in the past to facilitate circuit simulation in Spice [9–13]. However, in most cases the models are tested against results from device simulators instead of experimental devices [9,11,14–18]. This is likely due to the fact that most experimental results deviate substantially from ideal device simulations and do not produce sub-thermal switching behavior. Therefore there is a clear disconnect between experimental results and compact models and the realistic potential of TFET based circuits is still unknown.

In this paper, we address this disconnect by developing a physics based compact model that (1) fits experimental data, (2) explains the physics of non-idealities with compact expressions and (3) describes circuit performance for different levels of non-idealities and therefore lays a pathway for studying low power circuits based on TFETs. The main reasons of non-ideal switching behavior in TFETs is the existence of interface traps and non-abrupt density of states (Urbach tail) at the band edges. In the past we developed numerical models explaining the impact of trap assisted tunneling (TAT) [19] and how, combined with non-abrupt Urbach tail, it increases the sub-threshold swing of TFETs. In this paper, we present compact expressions of TAT based on Shockley-Read-Hall formalism. We also present simple expressions of channel potential and electric field and explain how they capture the details of TFET device physics such as the TFET quantum capacitance, super-linear output current and current saturation mechanism. We implement the model in Verilog-A and present TFET based inverter and oscillator circuit performance based on existing TFET data. The paper is organized as follows: Section II gives a brief overview of the impacts of TAT and the compact expressions of current from TAT. Section III describes the electrostatic model and Section IV describes the BTBT model that includes the Urbach tail. In Section V, we provide model fits to experimental data. The final Section (VI) describes the circuit simulation results using the compact model in Verilog-A.

2. Trap assisted tunneling model

Fig. 1 shows the device structure of a top-gate TFET and the position

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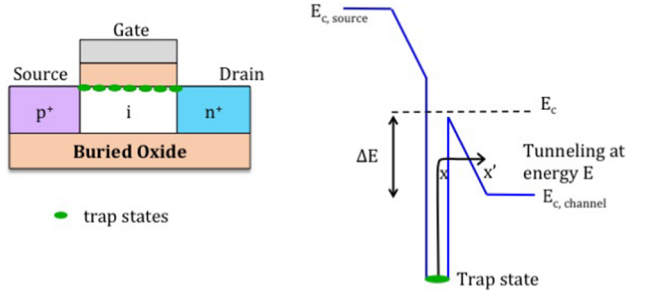

Fig. 1. (a) We consider the interface traps between the gate oxide and the channel. Although traps exist throughout the interface, substantial trap assisted tunneling (TAT) takes place only in the region where the electric field is high (source-channel junction). TAT can be of any combination of thermal emission (vertical transition along energy axis) and tunneling (horizontal spatial transition) as shown.

of the traps. The trap assisted tunneling is only strong where the electric field is high, in this case the source-channel junction. Below the threshold voltage, V_t (when BTBT is triggered), electron excitation by a phonon from the valence band to a trap state followed by tunneling into the conduction band (Fig. 1b) can give rise to leakage current. The problem is to find how much is the leakage floor compared to the BTBT current and how the overall sub-threshold swing is affected. Under high electric field, we have substantial band bending at the source-channel junction and in addition to thermal emission, electrons can partially be excited by phonons and then tunnel into the conduction band via tunneling. The overall process can be quantified by the original transition rate (e_{n0}) times an enhancement factor due to tunneling. The new rate becomes, $e_n = e_{n0} \times \Gamma$, where Γ accounts for the tunneling process. At energy E, the emission probability is enhanced since electrons are emitted into a lower energy level (E_c) than they would normally emit to. The emission rate is therefore enhanced to $e_{n0}\exp((E_c - E)/(k_B T))$ [20]. Accounting for the transmission probability (Tr) through the triangular barrier (from x to x') and integrating over the energy range ΔE, Γ is calculated as [21],

$$\Gamma_{n,p}(x) = \frac{1}{k_B T}\int_{E_c-\Delta E_{n,p}(x)}^{E_c} \exp\left(\frac{E_c - E}{k_B T}\right) Tr(E)\,dE \tag{1}$$

E is the energy to which the electron (or hole) is tunneling to (Fig. 1b). It can be shown,

$$\Gamma_{n,p}(x) = \frac{\Delta E_{n,p}(x)}{k_B T}\int_0^1 \exp\left[\frac{\Delta E_{n,p}(x)}{k_B T}u - K_{n,p}u^{3/2}\right]du \tag{2}$$

where $K_{n,p} = \frac{4}{3}\frac{\sqrt{2m^*_{n,p}\Delta E^3_{n,p}}}{q\hbar\mathscr{E}}$, defines the range of energy to which the electron (or hole) can tunnel to and from the trap. The subscript (n, p) indicates that the equations are equally applicable to both electron and holes.

Once Γ is calculated, the current can be obtained from the net generation rate following the same method as the conventional SRH formalism,

$$G^n(x) = \int \frac{n_i^2 - np}{\tau_p\frac{n+n_1}{1+\Gamma_p(x)} + \tau_n\frac{p+p_1}{1+\Gamma_n(x)}} D_{it}\,dE \tag{3}$$

$$I = qW\int G^n(x)\,dx \tag{4}$$

where n_i is the intrinsic carrier concentration, n and p are the electron and hole densities and τs are the minority carrier lifetime. With $\Gamma = 0$, Eq. (3) reduces to the conventional SRH formalism.

2.1. Compact expression of TAT

Eq. (2) involves integration and therefore is not suitable for circuit simulation. Assuming that lifetimes and electric field enhancement factors are the same for electron and hole, and that the channel is depleted of free carriers ($n = p = 0$) near the source-channel junction where most of the generation takes place, and constant generation rate over a length d_{gen}, we can simplify the above formalism into a compact form as below,

$$I_{TAT} = qW\frac{n_i}{2\tau}\Gamma d_{gen}\left[1 - e^{-\frac{qV_{DS}}{k_B T}}\right] \tag{5}$$

The integration over energy is eliminated because only the midgap traps contribute significantly to the TAT. From the SRH formalism, the carrier lifetime is given by, $\tau = \frac{1}{\sigma v_{th} D_{it}}$, where σ is the carrier capture cross section, v_{th} is the carrier thermal velocity [20] and D_{it} is the density of traps.

Typical channel electric field in TFETs vary around 1 MV/cm. In this high electric field regime ($K < 2/3\Delta E/(k_B T)$), the Γ expression can be simplified as following [21],

$$\Gamma = \frac{\Delta E}{k_B T}\sqrt{\frac{2\pi}{3K}}\mathscr{F}e^{\left[\frac{\Delta E}{k_B T} - K\right]} \tag{6}$$

where we use $\mathscr{F}$ as a fitting parameter. Thus Γ depends on the temperature T, electric field $\mathscr{E}$, and the material parameters effective mass (m^*), bandgap (E_g). Fig. 2 shows the comparison of the calculation of Γ from Eqs. (2) and (6) at room temperature, assuming $\Delta E = 0.4$ eV, $m^* = 0.04m_0$. The compact expression (Eq. (6)) shows good agreement with the exact numerical calculation (Eq. (2)) above $\mathscr{E} = 2 \times 10^7$ V/m with $\mathscr{F} = 2$. However, Γ in Eq. (6) represents an average enhancement factor over the entire generation volume (where the TAT takes place) and thus ΔE loses its direct physical meaning.

3. Electrostatics model

The TFET surface potential is strongly influenced by the drain voltage since the channel is primarily populated with drain injected carriers. At low drain bias, the carrier injection is high and therefore the channel potential is pinned due to high quantum capacitance. At the high drain bias limit, the injection is low and the potential is controlled primarily by the gate voltage. Fig. 3 shows the surface potential calculation of a silicon TFET from a self-consistent numerical simulation as done in [19]. In this work, we capture the surface potential including these effects with the following empirical compact expression,

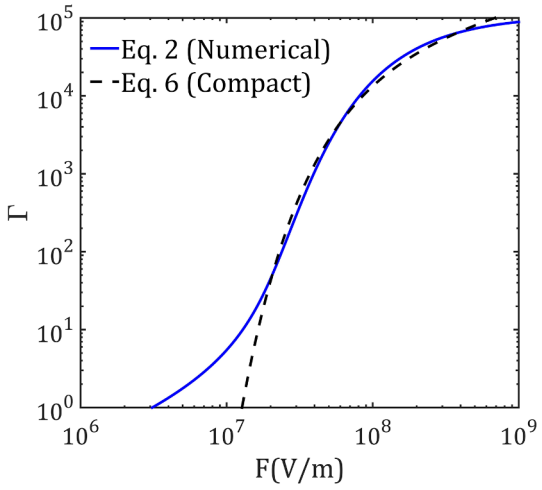

Fig. 2. Γ represents the enhancement in carrier generation (compared to classical SRH formalism) due to trap assisted tunneling. Since tunneling is electric field dependent, Γ changes with the electric field. This figure shows the accuracy of the compact expression of Γ (Eq. (6)) vs. the exact numerical calculation (Eq. (2)).

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