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An efficient redundant binary adder with revised computational rules☆

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ABSTRACT

Redundant binary representation (RBR) offers a carry-free addition of two redundant binary (RB) numbers. The computational rules of the conventional RB adder (CRBA) generate intermediate sum and carry vectors in RBR, leads to area overhead and pre-hardware elements for reverse conversion (RC). We have considered that the intermixing of inverted encoding of negabits (IEN) representation and conventional binary bits or posibits can be realized using standard hardware blocks. This paper provides a new computational rule for RB adder generating the intermediate sum and intermediate carry in posibit and IEN representations replacing the redundant digits. Thus, the proposed RB adder provides a single stage RB adder omitting the requirement of intermediate RB digits. For circuit synthesis of the proposed designs, we have considered Encounter® RTL Compiler and Xilinx Synthesis Technology in ASIC and FPGA platforms respectively. The comparative study of proposed NRBA offers improved design parameters as compared to CRBA.

1. Introduction

The addition and multiplication operation are the two vital computational blocks considering applications of digital signal processing (DSP). Each multiplication operation can also be considered as repetitive addition operations. However, the large carry propagation is the most challenging subject of research for computation of both addition and multiplication. Further, the implementation cost, power consumption and speed of all arithmetic operations are typically affected mainly by the choice of number representation and the computational algorithms [1]. The hardware implementation for the addition of the signed-magnitude numbers needs magnitude comparator along with a distinct subtraction unit. The computation is also needed pre and post complementation steps which add additional delay to the entire system. The other approach of signed-digit representation is done through redundant binary (RB) number system.

Redundant binary representation (RBR) is also preferable for designing high-performance multipliers, due to its high modularity and property of carry-free addition [1]. One of the essential blocks of a RB multiplier is RB partial products (PPs) reduction tree consisting of a group of RB adders [2,3]. As discussed, the carry propagation associated with addition operation is the major area of concern, the property of redundancy in RB number system is beneficial for limiting carry propagation for the addition of RB numbers. RB representation (RBR) is one of the cases of the signed digit (SD) number representation (SDR). In [4], Robertson presented that there are only nine different way to denote three values {$\bar{1}$, 0, 1} to

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two binary digits using permutation and negation operation. In [5,6], authors have determined the logical structure of a class of redundant adder with limited carry. Since then many researchers have been exploiting the assets of a RB number system to improve the overall speed of digital arithmetic.

The conventional RB adder (CRBA) offers to carry restricted addition operation, consisting of two stages of operations. The stage I of computation provide midway sum (Is) and midway carry (Ic) in RBR as per the computational rules. The computational rules of stage I include the logic design for an appropriate choice of Is and Ic, if there is any prospect of positive or negative carry to succeeding weighted digit position. Here, the ($Ic_i \in \{\bar{1}, 0, 1\}$) and sum ($Is_i \in \{\bar{1}, 0, 1\}$ at position 'i' are generated in such a way that $P_i + Q_i = 2Ic_i + Is_i$, where P_i and Q_i are considered as two RB digits. The RB adder is the optimum solution for carry propagation; however, this leads to problems related to the area overhead and large power consumption [7]. These two difficulties are primarily due to the necessity of at least two binary bits for representation of single RB digits and requirement of extra stage (stage II) of addition [1, 8]. Although, the logic design of the RB adder cell is reformed with the encoding style of RB digit i.e. sign–magnitude (SM), positive–negative (PN), and positive–negative complement (PNC) encoding [9–11], the computational rules of the RB adder remained same.

In our previous work [12], we have suggested a modified RB adder (MRBA) with less area utilization by reducing the number of intermediate stages of operations of CRBA. To achieve this, we have revised the traditional rules of the RB adder to minimize the addition operation to a single stage. We have measured IEN representation [13–15] as a potential alternative for signed number representation and the ability to realize hardware only using standard blocks. In case of proposed RB adder we have revised the computational rules of CRBA. For MRBA, the final result (positively weighted bit (m_i^+) and a negatively weighted bit (m_i^-) of RB digit) is obtained in pair of conventional binary (CB) and IEN bits instead of RB digits in case of CRBA. The resource utilization of MRBA is minimized over CRBA by performing addition operation in single stage eliminating the requirement of midway RB result. Therefore, the proposed MRBA omits the requirement of binary bits for intermediate RB digits resulting area efficient design. However, the logic design of MRBA is dependent on digits values at *ith* as well as $(i-1)th$ positions. Due to this, the proposed MRBA is having a higher delay as compared to CRBA. This paper is intended for further improvement over the MRBA reported in [12], by suggesting a new RB adder (NRBA). The logic design of the NRBA is revised as the generation of midway sum and carry are only dependent to next lower digit positions with single stage operation same as MRBA. Finally, it is believed that the proposed RB adder may set a fresh beginning for future research for RB designs.

The rest of the paper is organized as follows: Section 2 discusses the background of the redundant number system. Section 3 describes the proposed RB adder with revised computational rules. Section 4 provides the result and discussion of the proposed NRBA. The article concludes in Section 5.

2. Backgrounds on redundant binary (RB) number system

Avizienis defined the class of signed digit number system with symmetric digit sets $[-\alpha, \alpha]$ and radix $r > 2$ in the year 1960 [16]. Here, the value of α is restricted to $r/2+1 \le \alpha \le r-1$. Later, the redundant number systems with general asymmetric digit sets $[-\alpha, \beta]$ and lower redundancy with $r=2$ are discussed as generalized signed-digit (GSD) numbers system [17,18]. For example, the lower redundancy as binary signed digit (BSD) representation with $r=2$ and digit set $[-1, 1]$ is not covered by Avizienis. In GSD number system, the redundancy index (ρ) is defined as $\rho = \alpha + \beta + 1 - r$ and based on the value of 'ρ' the redundant and non-redundant positional number system are classified.

2.1. RB number system

This paper is mainly emphasized on redundant binary representation with minimal GSD ($\rho = 1$) with $\alpha = \beta$, i.e., symmetric minimal GSD, i.e. BSD. The BSD is also recognized as a redundant binary (RB) number representation. A n-digit RB number can be denoted as $\{y_{n-1}\, y_{n-2} \ldots y_1 y_0\}$ where y_i represents a radix-2 signed digit which belongs to the digit set i.e. $\{\bar{1}, 0,1\}$ and has the value of $\sum_{i=0}^{n-1} y_i * 2^i$ alike the unsigned integers representation but the difference is here y_i can also have value '$\bar{1}$'. Over the last few decades, RB number has developed as a vital representation format for the intermediate stage of parallel multiplier accumulating PPs.

Redundant binary number representation (RBR) is the special instance of signed-digit number representation (SDR). Let '*L*' be the range of number and '*V*' be the set of representation having interpretation function '*U*', so for SDR

$$U_{sdr} : V_{sdr} \rightarrow L_{sdr}$$

For SDR, $K_{sd} = \{K' \in K: -\alpha \le k \le \beta\}$, where K indicates to the set of digits and α, β should be greater than 0. The values of α and β states redundancy index (ρ) and redundancy is only exist if, $\alpha + \beta + 1 \ge x$. The range of number for SDR (L_{sdr}) can be termed as:

$$L_{sdr} = \left[-\alpha * \frac{x^n - 1}{x - 1}, \beta * \frac{x^n - 1}{x - 1}\right] \cap K$$

where x= radix size and n = MSB of the number.