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Design and implementation of a three-level active power filter for harmonic and reactive power compensation

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ABSTRACT

This paper presents a unified design and implementation of active power filters (APF) for medium-voltage high-power applications. A fast and accurate harmonic extraction technique based on the time transformation algorithm (TTA) is developed. A novel approach is used to derive the mathematical model describing the relation between the output current and the control signal of the NPC inverter for active power filter. Accordingly, the current controller and voltage controller are designed using the derived model. The neutral-point voltage is maintained near zero using a feed-forward controller. The designed three-level APF is feasible to implement, comparatively cheaper and reduces the filter size. From both the simulation and experimental results, it is found that the developed system provides excellent performance in regulating voltage and reducing harmonics significantly, from 26.3% to 4.0%.

1. Introduction

Industrial loads are predominantly composed of nonlinear loads in the form of frequency changers, motor drives and power converters. These are the main sources of harmonic pollution in grids, resulting in poor efficiency, a degraded power factor and can damage a equipment connected to the grid. The active power filter (APF) gives the most promising solution to compensate for the adverse effects of harmonics and reactive power simultaneously by using suitable control algorithms [1–5]. Different configurations of APF are available on the market for commercial use, and among them a shunt APF is widely used. The shunt APF (SAPF) is connected in parallel with the source and the load, injecting harmonics of opposite polarity to those present in the load current at the point of common coupling (PCC).

In the low-voltage field, there are already lots of well-rounded APF products below 690 V. However, in the high-voltage and high-power fields, the traditional two-level APF cannot fulfil their requirements because of the shortcomings of power switches as high-voltage semiconductor switches are still being remedied. A multilevel converter can be used as an alternative high-voltage switching device for high-power medium-voltage applications [6]. In addition, a multilevel converter has the advantages of low loss, low electromagnetic interference and low waveform distortion, and has become the new direction of development for active power filters [7–10].

The use of an APF at medium and high voltages is limited due to semiconductor's reverse-voltage rating constraint, high losses caused by switching high voltage and high current and high *dv/dt* generating electro-magnetic interference (EMI) as well as insulation degradation in electronic and electrical systems. An APF can be used in high-voltage applications, but comes with issues like losses, unreliability, complex control structure, high cost and a surge over-voltage problem. Another alternative is a cascaded connection of two PWM (pulse-width modulation) VSIs (voltage source inverters) with different power rating and switching frequency. This reduces the switching stress and commutation loss but the overall cost and size of the equipment goes up.

Multilevel inverters with different topologies have been developed for medium voltages and high-rated power applications to cover up the deficiencies of the above alternatives [11]. Neutral point clamped [12], flying capacitor [13], and cascade half-bridge [14] are the three most common topologies in multilevel inverters. The authors in [15] presented a comprehensive comparison of these three topologies. In an active power filter for commercial application, the cost, size and reliability of the system are of prime importance. The cost and size of capacitors are greater than diodes and the failure rate is higher in capacitors than diodes. In real power conversion cascaded H-bridge (CHB) requires an isolated dc source, but not in APF, however there are many voltage variables that need to be controlled in the case of APF which makes its control more complex. Therefore, NPC is selected owing to

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the application requirements and the ease of design and implementation as proposed in [16].

Current harmonic extraction technique plays a crucial role, especially in feedforward harmonic detection control structure determining speed and accuracy of APF [17,18]. Reference current extraction is carried out in two domains, frequency (fast Fourier transform (FFT), discrete Fourier transform (DFT)) and time (p-q, synchronous d-q, etc.). Time-domain techniques are preferred over frequency-domain techniques owing to their faster response and simplicity in real-time implementation [19,20].

As the APF needs to generate non sinusoidal currents, the design and implementation of the current controller is very demanding. Various control techniques like proportional-integral (PI), hysteresis, proportional-resonant (PR), and advanced and intelligent control have been proposed and used [21–23]. PI is still preferred due to its simpler implementation, and its performance conforms to the grid requirements [24]. The topological structure (NPC inverter) brings an unbalance of neutral-point voltage which is addressed using a feed-forward controller [25].

There has been a considerable interest in the use of a three-level inverter for APF but very few studies are available interlinking the various stages of implementation. This paper aims to bridge that gap by focusing on different stages of implementation. A unified complete control structure, consisting of harmonic current detection method, current control, DC-voltage control and neutral-point voltage control, for the APF with a three-level NPC converter is developed and implemented. A novel and simple approach for deriving mathematical model of three level NPC inverter is proposed in the paper. Compared to the previous approaches, the proposed modelling utilizes state space averaging method. The derived model simplifies the controller parameter design procedure and are used to design optimal control parameters for inner current and outer voltage control loop. The accuracy and performance of the derived model is verified through simulation and experimental results. Parameters of the power circuit are determined mathematically which ensures the optimum performance of the designed APF. The designed system accurately detects the harmonic and reduces to acceptable level. Finally, the simulation results are verified by experimental results to validate the efficacy of the proposed methods.

The paper is organized into four sections. Section 2 provides a brief review of APF principles and power-circuit parameter design. The control subsystem, consisting of a harmonic detection mechanism and voltage and current controller design, is discussed in Sections 3 and 4. The simulation and experimental results are presented in Sections 5 and 6. Section 7 presents a summary of this paper.

2. Power-circuit parameter design

There are three main power-circuit parameters to be calculated: (i) reference value of DC-side voltage; (ii) output filter inductor; and (iii) DC-side capacitance. The DC-link voltage should be at least greater than the peak of the line-to-neutral voltage to realize the compensation characteristics. The voltage rating of the switching devices is given by:

$$V_{\text{device-rating}} \times (m-1) \geq 2V_{\text{ll}}, \quad V_{\text{device-rating}} \geq V_{\text{ll}} \tag{1}$$

where $m = 3$. The performance of an APF depends upon the selection of capacitor's value; the DC-side voltage should be constant for good compensation. Unlike in a two-level inverter, the voltage rating of the capacitors is reduced in a three-level inverter and is half of the DC-side reference voltage. During compensation the voltage of the capacitor fluctuates, and the fluctuation is a function of the capacitance and the reference DC-side voltage. Higher fluctuations will degrade the compensation performance while lower fluctuations require a higher capacitance, which increases the size and cost. Hence it should be limited to within a pre-specified value by selecting a suitable capacitance which can be determined as [26]:

$$C \geq \frac{3E_m I_m}{2\varepsilon\omega V_{\text{dc}}^2} \tag{2}$$

where E_m is the grid peak voltage, I_m is the output nominal current, ε is the DC voltage fluctuation component which is taken 10%, ω is grid angular frequency and V_{dc} is the dc side voltage. The output inductor provides an interface of the APF with the electrical system as well as filtering out the high-frequency switching ripples of the inverter output AC current. In general, the larger the value of the inductor the betters the suppression of switching ripple, but with poor current tracking and larger size, cost will be higher. In comparison to a two-level inverter, the output voltage of a 3-level inverter is more like a sine wave, hence the filtering requirement is reduced. The inductor's value is determined based on the maximum ripple allowed in the output current [27] and given as:

$$L_a \geq \frac{(\text{Vdc}/2)(1-|D|)|D|\ T_s}{2\Delta I_{L\max}} \tag{3}$$

where $\Delta I_{L\max}$ is the maximum ripple current in one switching cycle, D is the duty cycle and T_s is the switching time period. From the above equation it is clear that L_a has maximum value when $(1 - |D|) = |D|$.

3. Current reference estimation

The generalized structure of a three-phase shunt APF with a three-level NPC inverter is shown in Fig. 1. The power stage consists of a three-level NPC VSI behaving as a current source, connected in parallel at the point of common coupling (PCC). The load current is sensed and the harmonic content present in it is extracted, serving as a reference compensation current for the inner current control loop. The current control loop ensures that the APF generates a reference current to achieve the desired compensation. A voltage control loop is essential to maintain the DC-side capacitor voltage to a reference value against the losses in the VSI.

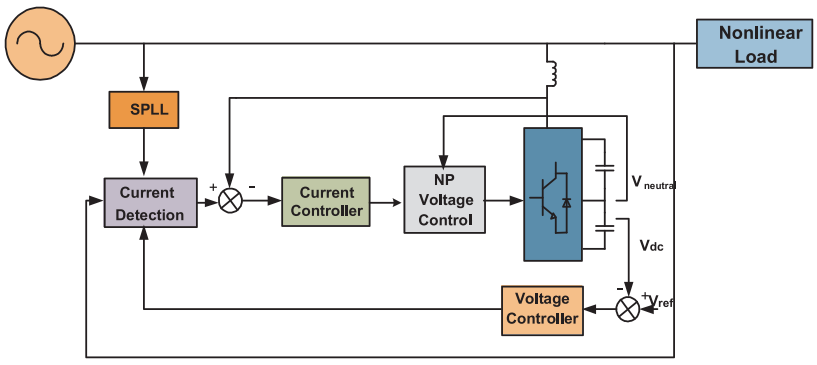

Fig. 1. General control structure of APF with 3-level NPC inverter.