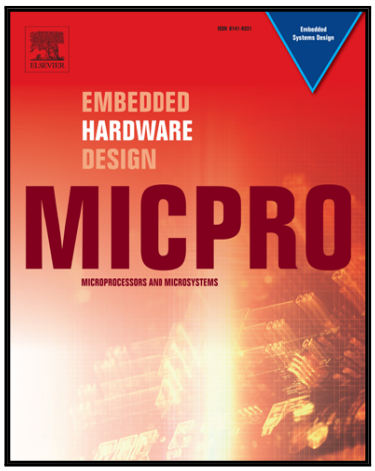

Code-design for efficient pipelined layered LDPC decoders with bank memory organization

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Code-design for efficient pipelined layered LDPC decoders with bank memory organization

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Abstract

This paper presents an architecture-aware Progressive Edge Growth (PEG)-based construction method for Low-Density Parity-Check (LDPC) codes. We target optimization through code construction for layered architectures with pipelined processing and memory organized in single-port banks. For a given layered Quasy-Cyclic Low-Density Parity-Check (QC-LDPC) decoder architecture configuration, the code constraints need to maximize hardware usage efficiency. Implementation results for Field-Programmable Gate Array (FPGA) technology suggest that the codes obtained using the proposed algorithm have a throughput increase of 39% up to 110%, due to the increase in working frequency obtained by using pipeline.

Keywords: Parity check codes, Decoding, Channel coding, Progressive Edge Growth, Layered, Graph Coloring, Architectures

1. Introduction

A key objective in the development of LDPC decoding architecture is to obtain the maximum throughput, given a fixed resource budget. This goal