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Embedding hypercubes and folded hypercubes onto Cartesian product of certain trees

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A B S T R A C T

The hypercube network is one of the most popular interconnection networks since it has simple structure and is easy to implement. The folded hypercube is an important variation of the hypercube. Interconnection networks play a major role in the performance of distributed memory multiprocessors and the one primary concern for choosing an appropriate interconnection network is the graph embedding ability. A graph embedding of a guest graph G into a host graph H is an injective map on the vertices such that each edge of G is mapped into a path of H. The wirelength of this embedding is defined to be the sum of the lengths of the paths corresponding to the edges of G. In this paper we embed hypercube and folded hypercube onto Cartesian product of trees such as 1-rooted complete binary tree and path, sibling tree and path to minimize the wirelength.

1. Introduction

The problem of efficiently implementing parallel algorithms on parallel computers has been studied as a graph embedding problem. The computational structure of a parallel algorithm A is represented by a graph G_A and the interconnection network of a parallel computer N is represented by a graph H_N. An embedding of G_A into H_N describes the working of the parallel algorithm A when implemented on N [1]. Such a simulation problem can be mathematically formulated as follows: Given a guest graph G and a host graph H. An embedding of G into H is an ordered pair $\prec f, P_f \succ$, where f is an injective map from $V(G)$ to $V(H)$ and P_f is also an injective map from $E(G)$ to $\{P(f(u), f(v)) : P(f(u), f(v))$ is a path in H between $f(u)$ and $f(v)$ for $(u, v) \in E(G)\}$ [2–5]. See Fig. 1. An edge congestion of an embedding $\prec f, P_f \succ$ of G into H is the maximum number of edges of the graph G that are embedded on any single edge of H. Let

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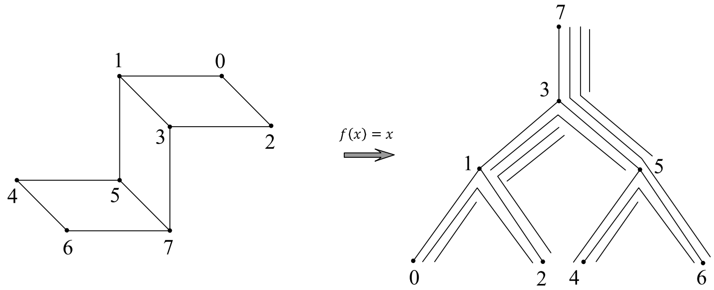

Fig. 1. Embedding the wiring of a ladder into the 1-rooted complete binary tree with $f(x) = x$ and $P_f(0,1) = (0,1)$, $P_f(0,2) = (0,1,2)$, $P_f(1,3) = (1,3)$, $P_f(1,5) = (1,3,5)$, $P_f(2,3) = (2,1,3)$, $P_f(3,7) = (3,7)$, $P_f(4,5) = (4,5)$, $P_f(4,6) = (4,5,6)$, $P_f(5,7) = (5,3,7)$, $P_f(6,7) = (6,5,3,7)$.

$EC_{\prec f,P_f \succ}(e)$ denote the number of edges (u,v) of G such that the path $P(f(u),f(v))$ contains the edge e in H [6]. In other words, $EC_{\prec f,P_f \succ}(e) = |\{(u,v) \in E(G) : e \in P(f(u),f(v))\}|$.

The performance of an embedding can be measured by dilation, expansion and edge congestion sum (wirelength). The dilation of an embedding $\prec f, P_f \succ$ is defined as $dil_{\prec f,P_f \succ}(G,H) = \max\{|P(f(u),f(v))| : (u,v) \in E(G)\}$. The smaller the dilation of an embedding is, the shorter the communication delay that the graph H simulates the graph G. The expansion of an embedding $\prec f, P_f \succ$ is defined as $Exp_{\prec f,P_f \succ}(G,H) = |V(H)| / |V(G)|$. Expansion measures the processor utilization. The smaller the expansion of an embedding is, the more efficient the processor utilization that the graph H simulates the graph G [7].

Combinatorial isoperimetric problems arise frequently in communications engineering, computer science, physical sciences and mathematics. Layout problems arise in electrical engineering when one takes the wiring diagram for some electrical circuit and lay it out on a chassis. A wiring diagram is essentially a graph, the electrical components being the vertices and the wires connecting them being the edges [8]. See Fig. 1.

The wirelength [6,8] of an embedding $\prec f, P_f \succ$ of G into H is given by

$$WL_{\prec f,P_f \succ}(G,H) = \sum_{(u,v)\in E(G)} |P(f(u),f(v))| = \sum_{e\in E(H)} EC_{\prec f,P_f \succ}(e).$$

The minimum wirelength of G into H is defined as $WL(G,H) = \min WL_{\prec f,P_f \succ}(G,H)$ where the minimum is taken over all embeddings f and P_f of G into H.

Embedding problems have been considered for binary trees into hypercubes [9–16], binomial trees into hypercubes [17,18], generalized ladders into hypercubes [19,20], hypercubes into cycles [21,22], hypercubes into grids [6,23,24], hypercubes into cylinders, snakes and caterpillars [25], hypercubes into certain trees [26], m-sequential k-ary trees into hypercubes [27], folded hypercubes into grids [28] and complete binary trees into folded hypercubes [1].

Among the interconnection networks of parallel computers, the binary hypercube has received much attention. An important property of the hypercube which makes it popular, is its ability to efficiently simulate the message routings of other interconnection networks and hence becomes the first choice of topological structure of parallel processing and computing systems. The machine based on hypercubes such as the Cosmic Cube from Caltech, the iPSC/2 from Intel and Connection Machines have been implemented commercially [1]. For $n \geq 1$, let Q_n denote the n-dimensional hypercube. The vertex set of Q_n is formed by the collection of all n-string binary representations. Two vertices $x, y \in V(Q_n)$ are adjacent if and only if the corresponding binary representations differ exactly in one bit [5]. Equivalently if $|V(Q_n)| = 2^n$ then the vertices of Q_n can also be identified with integers $0, 1, \ldots, 2^n - 1$ so that if a pair of vertices i and j are adjacent then $i - j = \pm 2^p$ for some $p \geq 0$. An incomplete hypercube on i vertices of Q_n is the graph induced by $\{0, 1, \ldots, i-1\}$ and is denoted by L_i, $1 \leq i \leq 2^n$ [29]. See Fig. 2.