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Experimental evaluation of micro-ion trap mass spectrometer geometries

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ABSTRACT

We describe a new fabrication method, simulations, and experimental results for micromachined cylindrical ion trap (μ-CIT) arrays for use in miniaturized mass spectrometers. The micromachined μ-CIT arrays were fabricated in a silicon-on-insulator (SOI) substrate, and a variety of trap geometries were incorporated into a single μ-CIT array chip to allow fast iterative measurements of the differences in the mass spectra from μ-CITs with different ratios of half-axial to half-radial dimensions (z_0/r_0). The chip dimensions were approximately 1.0 cm × 1.5 cm × 0.1 cm. A series of z_0/r_0 were chosen in incremental steps of 3% for each array by changing r_0 from 308 to 392 μm while keeping z_0 fixed at 355 μm, resulting in a range of z_0/r_0 from 1.16 to 0.92 (nine geometries in total). Simulations were performed in SIMION 7.0 to determine the optimum range of μ-CIT z_0/r_0 to be fabricated and tested, by producing simulated mass spectra from μ-CITs with a variety of z_0/r_0 to evaluate predicted mass resolution. Following the simulations, we fabricated the arrays of μ-CIT geometries in SOI wafers using deep reactive ion etching (DRIE) to create the cylindrical structures and surface metallization to create ion trap electrodes. Symmetrical arrays of half-CITs were fabricated, diced, and bonded back-to-back to obtain complete μ-CIT array chips containing all nine geometrical ratios (z_0/r_0), which are referred to in this paper as the “gradient arrays”. The bonding process provided approximately 5-μm alignment accuracy between the two arrays of half-CITs, and the resulting arrays had flat μ-CIT endplate electrodes with <3 μm upwards bow. We discuss several critical issues encountered during process development such as delamination of the buried oxide layer, excessive wafer bow, high capacitance, and ring-electrode wall verticality, along with solutions to mitigate these issues. Mass spectra were obtained experimentally from each trap geometry, and μ-CIT performance was found to follow the trend with respect to z_0/r_0 observed in the simulations. Experimental efforts indicated that axial modulation on one endplate electrode was required to remove spurious peaks in the mass spectra (caused by higher-order multipole contributions to the trapping electric field), and resulted in mass spectra with full-width-at-half-maximum peaks of 0.4 amu.

1. Introduction

It is important to develop low-power, potentially handheld, high-performance chemical analyzers to monitor and characterize naturally occurring and man-made chemicals, their (re)distributions and transformations [1]. Mass spectrometry has evolved as a powerful and versatile chemical analysis tool, and has been tailored to fit a broad spectrum of applications. These applications range from laboratory-based clinical measurements, drug testing, analysis of food products, pharmaceutical screening measurements, and environmental chemical analysis. There has been much activity to miniaturize MSs for prolonged in situ measurements at remote or hazardous locations, where it is costly for humans to collect samples and deliver to a laboratory for analysis [2]. For example, field-deployable mass spectrometers (MSs) have been used for in situ measurements of ocean chemistry [3,4], offsite volcanic monitoring [5], space explorations for biogenic chemical compounds that could indicate extraterrestrial life [6], and studies of comet chemical compositions [7,8].

Most commercially available portable MS systems are somewhat miniaturized and ruggedized versions of conventional, laboratory-style instruments, which have been tailored for in situ chemical analysis. Further miniaturization based on current technologies gets increasingly difficult, and calls for radically different design methods and new integration approaches for very small components. Such approaches are necessary to

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significantly reduce the footprint of all the components, the vacuum housing, and the electronic circuits. Ion trap MSs are a good choice for miniaturization because of their inherent tolerance to relatively high pressures, and because of their scalability without degradation of mass spectral resolution compared to other types of mass analyzers, such as time-of-flight (TOF) MSs and double-focusing sector MSs [9]. Bonner et al. [10] studied the trapping performance of cylindrical ion traps, finding them to generate an effective electric trapping potential quite similar to that of quadruple ion traps (QITs) with hyperbolic electrodes. Thus, for ease of machinability, some groups have chosen to use cylindrical ring electrodes instead of hyperbolic ones, and have demonstrated a similar potential distribution [11] and device performance [12] for certain radius-to-length ratios (r_0/z_0) [13]. It has been shown that as the r_0 of an ion trap is reduced, the corresponding RF voltage required on the ring electrode to scan out an ion drops as the square of the radius, if the RF frequency is held constant. And for a given trap capacitance, the power required drops by the square of the RF voltage. For very small traps, however, the effective potential well depth becomes too small at very low voltages, so the frequency is typically increased to allow operation at higher voltages, and the overall power consumption is increased accordingly [14]. Still, a tremendous power savings can be accomplished by using very small ion traps.

During miniaturization, however, geometrical imperfections, such as surface quality, alignment of the electrodes, and dimensional variations of miniature μ-CIT MSs, become relatively more prominent, significantly affecting the trap performance [15]. Therefore, it becomes increasingly important to fabricate these miniaturized structures with high precision. At the sub-millimeter scale, conventional machining of metals becomes less practical, especially for complex 3-D structures, and could be expensive, requiring special machining capabilities such as electrical discharge machining. For a variety of millimeter-scale mass analyzers, several less conventional machining methods have been investigated, such as stereo lithography of photosensitive resin to build rectilinear ion traps [16], photolithographically patterned metal surface electrodes on ceramic discs to build a halo ion trap [17], and compression molding of low-temperature co-fired ceramics (LTCCs) to build small CITs [18]. Each of these technologies offers a unique set of advantages over conventional machining, depending on the choice of substrate and mass analyzer.

Reducing the size of ion-trap-based MSs also results in lower ion storage capacity, which can lead to lower sensitivity or degradation in mass resolution due to space charge effects (i.e., Coulomb interactions of the ions) if the traps are overfilled. One recent study on the miniaturization of ion traps estimated the total number of analyzable ions scales as the 1.55–1.75 power of the CIT radius [19]. Several groups [20,21] have proposed building arrays of miniature CITs that can be operated in unison, to make up for the loss in sensitivity of a single miniaturized CIT. In addition, new capabilities offered by arrays of CIT MSs, such as parallel analyzes of chemicals, have been proposed and investigated [22].

Another technology that has been applied to achieve extreme miniaturization is microelectromechanical systems (MEMS), due to the ease of building extremely miniature structures with high precision. Components and subsystems of the MS system that have been built using micromachining technologies include sub-millimeter ion trap MSs [14,17,23–25], a surface microstructure miniature MS [26], time-of-flight analyzers [27], quadrupole mass filters [28,29], Wien filters [30], micro pumps [31], and small electron [32] and ion sources [33]. A complete MS system, fully integrated with the MEMS approach, has also been demonstrated to build a highly miniaturized chemical sensor [34]. The key advantage of the MEMS approach is that it offers high-precision structures and allows integrated assembly techniques that are not achievable by assembling machined metal components. High-aspect-ratio etching, such as deep reactive ion etching (DRIE) [35], can be used to produce 3-D structures (e.g., cylinders and trenches) in Si. A MEMS approach can ultimately be cost-effective through batch fabrication, as multiple micro-devices can be processed simultaneously on a batch of 100-mm diameter Si wafers. Monolithically designed ion trap structures could also offer extra mechanical ruggedness and higher alignment accuracy with less stringent assembly requirements [23].

CITs are an ideal candidate for miniaturization and microfabrication due to their relatively simpler geometry compared to quadrupole ion traps with hyperbolic electrodes. A wide range of μ-CITs with sizes of 1–700 μm r_0 have been micromachined over the past decade. One approach was to use iterative sputtering of tungsten to form the trap electrodes of ion traps with 1–10 μm r_0. These μm-scale traps were found to have very high capacitance due to close proximity of the trap electrodes [14]. Another group fabricated 20-μm r_0 ion traps in silicon; these traps successfully obtained a mass spectrum of xenon gas from an array [23].

We have investigated and reported on various substrates for fabrication of miniature CITs with high precision. Low-temperature co-fired ceramics [18], ceramics (alumina 99%), and Si wafers [24] are substrates that we have successfully used to construct miniature CITs. This article focuses on the fabrication and testing of a new μ-CIT array design in silicon-on-insulator (SOI) substrates, incorporating a variety of μ-CIT sizes (r_0/z_0) in each array. The design allowed for faster iterative testing to analyze the trap performance and to identify the optimum geometries. Here we report on the design, simulation, fabrication, and testing of these μ-CIT arrays.

2. Device design

The design approach adopted to create this generation of μ-CIT arrays is a derivative of our previous designs [24]. An SOI substrate was chosen instead of Si to: (1) incorporate a thicker endplate electrode for better mechanical ruggedness, (2) incorporate a thicker SiO_2 layer for lower capacitance and higher breakdown voltage, and (3) enable a simpler fabrication process. The wafers were custom ordered from Ultrasil and MEMS Engineering with a buried oxide layer (BOX) of 10 μm sandwiched between a 350-μm-thick Si layer (called “handle Si”) and a 40-μm-thick Si layer (called “device Si”). Fig. 1 illustrates the structural details of two chip-scale arrays of half μ-CITs that were bonded back-to-back to obtain a complete μ-CIT array. To fabricate a range of geometries (z_0/r_0) in the same SOI chip, a series of r_0 with a 3% increment in r_0 was incorporated into the mask design. Since the wafer thickness was constant for an SOI wafer, this resulted in a z_0/r_0 range (1.16–0.92). Each array consisted of nine columns of three identical traps to investigate the uniformity of MEMS structures and chip boundary effects. To investigate the effect of aperture size on the trapping performance, two sets of the gradient arrays (each with 3 × 9 traps) were incorporated within a single SOI chip: one with aperture size 30% of r_0 and the other with 45% of r_0. The overall footprint of each SOI chip was approximately 1 × 1.5 cm, and fabrication was performed using a 100-mm diameter SOI wafer. Table 1 lists the design details for each gradient μ-CIT array, where z_0 is the sum of handle Si wafer thickness (z_b) and the gap (d_s) between the ring and endplate electrode, while d_e is the endplate electrode thickness.

3. Simulations

Simulations were performed in SIMION 7.0 to determine the anticipated spectral quality of a range of trap geometries to guide