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A novel phase-coherent programmable clock for high-precision arbitrary waveform generation applied to digital ion trap mass spectrometry

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ABSTRACT

Digital ion trap (DIT) mass spectrometry requires the ability to precisely and accurately produce waveforms. The quality of the mass spectra produced in terms of resolution and mass accuracy depend on the resolution and precision of the applied waveforms. This publication reveals a novel method for the production of arbitrary waveforms in general and then applies the method to the production of DIT waveforms. Arbitrary waveforms can be created by varying the clock frequency input to a programmable read only memory that is then input to a digital-to-analog converter (DAC). The arbitrary waveform is composed of a defined number of points that are triggered to be written after programmed numbers of clock cycles to define the arbitrary waveform. The novelty introduced here is that the direct digital synthesis (DDS) generated clock frequency can be precisely changed as the arbitrary waveform is written because we have developed a method to rapidly switch the DDS frequency exactly at the end of the output clock cycle allowing exact timing of multiple transitions to produce precise and temporally complex waveforms. Changing the frequency only at the end of the output clock cycle is a phase-coherent process that permits precise timing between each point in the arbitrary waveform. This waveform generation technique was demonstrated by creating a prototype that was used to operate a digital ion trap mass spectrometer. The jitter in the phase-coherent DDS TTL output that was used as the frequency-variable clock was 20 ps. This jitter represents the realizable limit of precision for waveform generation. The rectangular waveforms used to operate the mass spectrometer were created with counters that increased the arbitrary jitter to 100 ps. The mass resolution achieved was 5000 at $m/z = 414$. Resolution should improve with increasing mass because the waveforms have longer periods while the jitter should remain constant. Given the current limit of the variable clock resolution, much better mass resolution should be achievable with future generations of the waveform production system. The agility of the DDS function generators permits the phase-coherent variable clock to be switched at a rate up to 250 MHz. This permits arbitrary waveforms to be produced with much more temporal complexity than previously possible.

1. Introduction

Digital ion trap (DIT) mass spectrometry has been developed in the last decade [1–3]. It has enormous potential for the analysis of large molecules and particulate ions because its mass range is essentially limited only by the ability to trap ions. Currently, inroads are being made in trapping particulate ions sampled from the atmosphere [4–6]. As these technologies come into use, the utility of DITs will increase.

One of the biggest problems in producing a DIT is the production and control of the digital waveforms. In general, DITs operate by scanning or stepping the frequency of the trapping and/or excitation waveforms. These frequencies must be changed rapidly to produce a mass scan. The correlation between the ejected mass and the waveform frequency is not a linear function [7]. Consequently, the waveforms must be scanned or stepped nonlinearly for the ejection mass to correlate linearly with time during a scan. DITs operate with rectangular waveforms. The stability region of the ions in the trap varies with the duty cycle of the trapping waveform [8]. Changing the duty cycle provides a quick method of mass selection. Modifying the duty cycle of the trapping waveform is equivalent to adding a DC component to the trapping field [8,9]. If a digitally operated linear quadrupole is used as a mass filter, the duty cycle sets the width of the mass window for the transmitted ions. Additionally, the duty cycle of the excitation waveform can be varied and its phase can be adjusted to optimize resolution [3]. Precise control of the waveforms in terms of frequency, amplitude, phase and duty cycle is extremely

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important to the practice of digital ion trap mass spectrometry.

When we started this project, a commercially available method for producing and changing the rectangular waveforms needed for DIT mass spectrometry did not exist. Ding et al. [3] produced the waveforms for their DIT using direct digital synthesis (DDS). They used a field programmable gate array (FPGA) to rapidly change the frequency of the waveforms and scan the mass spectrum. They also accomplished pulse width modulation of the excitation waveform (changing the duty cycle) with 8-bit control (1 part in 256). Pulse width modulation using DDS can be accomplished with an external DAC to set the level of the comparator used to create the rectangular waveform from the filtered sine output. Theoretically, duty cycle modulation can be accomplished with up to 16-bit control (1 part in 65,536) based on the resolution of the DAC used to control the comparator. Ideally, better precision and accuracy in producing the rectangular waveforms will yield better resolution and accuracy in digital ion trap mass spectrometry.

With this information, we set about creating an agile waveform generator. We decided to use DDS technology as the basis for our waveform generator because the frequency can be changed as fast as the phase word can be downloaded to the device and the waveforms can be generated with up to 48-bit frequency resolution. Upon reviewing the methodologies used to generate waveforms, we further decided that the best course was to use the DDS to create a frequency-variable clock that could be used to read out arbitrary waveforms.

The idea of writing an arbitrary waveform into programmable memory and then using a frequency-variable clock to read the waveform into a digital-to-analog converter (DAC) to create arbitrary waveforms is old. It is schematically depicted in Fig. 1. In the earliest versions, all of the waveform points within the memory were played out on each cycle and the frequency of the arbitrary waveform was defined by the frequency of the clock, $F_{arb} = F_{clock}/N$, where N is the number of points that define the arbitrary waveform. Memory segmentation and sequencing were rapidly developed to create more complex arbitrary waveforms requiring smaller amounts of memory. In these strategies, the variable clock defines all of the temporal characteristics of the arbitrary waveform.

Currently, many arbitrary waveform/function generators use DDS technology to create arbitrary waveforms and other functions. This technology uses an internal clock, a phase accumulator, memory for waveform storage or a look-up table, a DAC and a low-pass filter [10]. The greatest advantage of this technology is that it can provide frequency resolution to millihertz levels [11]. The disadvantages are waveform jitter and the lack of sequencing capability. Waveform jitter results from up or down sampling of the waveform when the frequencies are not equal to the clock frequency divided by the waveform length or submultiples. This results in missing samples and temporal jitter [10]. This disadvantage could be circumvented if the DDS-based waveform generator could be operated with an external variable clock; however an external signal cannot be used to clock out the waveform in typical commercial DDS waveform generators [12]. The inability to segment the memory and piece the segments together (sequencing) to create large waveforms without the use of massive amounts of memory also limits the complexity of the waveforms produced by direct digital synthesis.

More recently, waveform generators have been produced that permit the use of an external variable clock and permit sequencing to produce complex waveforms [12]. These generators can take advantage of the phenomenal frequency resolution of DDS by using it to generate the external clock signal. The limitation of this technique is that frequency of the clock cannot be changed during the production of the waveform. That is, the spacing of the points in the waveform cannot be changed once the clock frequency is set. DDS technology permits precise definition of the timing in the waveform provided that all of the required transitions in the waveform occur at integer increments of the DDS clock waveform period. If not, then the DDS clock frequency has to rapidly change during the creation of the waveform and the change has to occur consistently and predictably. Unfortunately, that is not possible with the current state of DDS technology.

Normal direct digital synthesis occurs as follows [10]. A 24–48-bit word defines the stepping of the phase of a sine wave in a phase accumulator. The phase is accumulated at a fixed frequency defined by a reference clock. The accumulated phase is referenced to a sine look-up table that defines the y-value of the sine as a function of phase. This y-value is then input to a DAC. The DAC steps through the y-values of the sine wave at a rate defined by the reference clock. The stepped sine wave from the DAC is then passed through a filter that removes the high frequency components to yield a smooth sine wave whose frequency and resolution is defined by the stepping of the phase rather than the reference clock frequency (see Fig. 2).

The frequency-switching process of the DDS can occur as fast as the word that defines the stepping of the phase can be downloaded to the DDS chip. This rate is defined by speed of the control interface and the loading configuration selected. Typically, DDS devices provide a parallel byte load to facilitate getting data into the control registers. Control data clocking rates of 100 MHz are generally supported for the byte load parallel control interface. This means that a new tuning word can be loaded to the DDS every 10 ns. Switching of the frequency can happen at any point in the phase accumulation and yield very different waveforms during the transition. To illustrate this point, we have plotted the accumulator, sine look-up and the comparator outputs from a DDS device for a factor-of-5 reduction in frequency that occurs at various points in the phase accumulation process in Fig. 3.

Consequently, the output waveforms during frequency stepping may be quite different. We call the fluctuations of the frequency

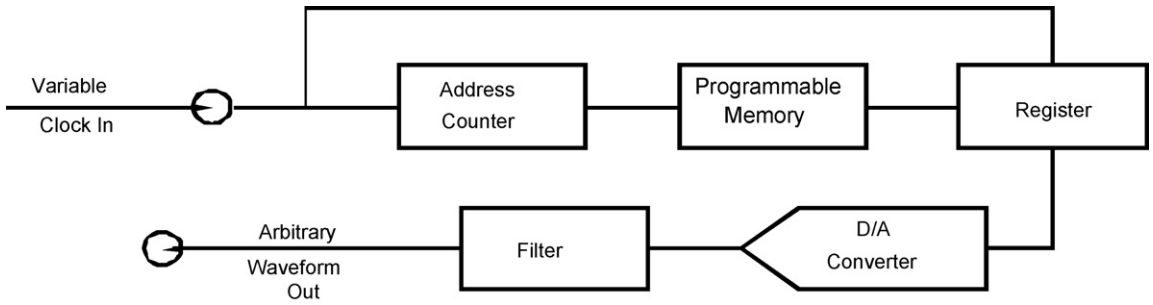

Fig. 1. A schematic depiction of arbitrary waveform generation with a variable clock. A waveform is written into memory. The frequency of a variable clock is then set to define the rate at which the points that define the amplitude of the waveform are read into a digital-to-analog converter to create the digital arbitrary waveform that is then passed through a low-pass filter to remove the high frequency components and create a smoothed arbitrary wave.