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Synergistic effect in organic field-effect transistor nonvolatile memory utilizing bimetal nanoparticles as nano-floating-gate

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ABSTRACT

A solution-processed bimetal nano-floating-gate, with a combination of stabilized Ag and Pt nanoparticles, is utilized to achieve high-performance organic field-effect transistor nonvolatile memories. The device based on the Ag–Pt nano-floating-gate shows the synergistic superiority in memory performance compared with the corresponding Ag-only and Pt-only devices. The Ag and Pt nanoparticles are found to prefer hole and electron trapping, respectively. Upon the blending of the Ag and Pt nanoparticles, both hole and electron trapping are significantly enhanced and thus realize a large memory window. The dipole enhancement induced local work function change for both Ag and Pt is proposed to be responsible for the synergistic effect, and this physical picture is supported by the electronic structure results. It is concluded that using a hybrid nano-floating-gate is a promising strategy to optimize the device performance of organic field-effect transistor nonvolatile memories.

1. Introduction

Organic nonvolatile memories based on organic field-effect transistors (OFETs) have attracted great attention in the field of organic electronics [1–3], which operate in advantageous manner of reliable data storage and nondestructive data reading. OFET nonvolatile memories are compatible with organic logic circuits, making themselves promising components for future flexible electronic applications. There are three typical approaches to modulate and maintain the channel conductivity in an OFET memory: (1) retainable polarization of a ferroelectric gate dielectric [4,5]; (2) charge trapping into a polymeric gate electret [6–8]; and (3) charge trapping into a floating-gate [9–16]. The floating-gate architecture is beneficial for getting good memory retention and endurance, owing to its isolation of carrier transport and charge storage layers with a tunneling dielectric in between. Especially, by adopting spatially discrete charge trapping sites, nano-floating-gate applied in an OFET memory can effectively suppress the charge leakage effect and hence improve device retention capability [11,14]. It is also in favor of scaling down the dielectric thickness, which is critical to reduce device programming/erasing bias [17]. Metal nanoparticles (NPs) have been often employed as nano-floating-gate, because their size, density and assembly could be tailored to optimize the memory performance [1,12]. Besides commonly used monometal nano-floating-gate, hybrid nano-floating-gate has been utilized as well and has shown superior performance compared with the unitary counterparts [18–20]. It is thus meaningful to probe the superiority of bimetal nano-floating-gate in OFET nonvolatile memories. Wei et al. report that the nano-floating-gate based on Ag and Pt NPs cause negative and positive threshold voltage (V_T) shifts in the OFET memories, respectively [21]. It is interpreted by the physical picture that Pt NPs mainly trap and confine electrons while Ag NPs mainly trap and confine holes, due to a large difference in their Fermi level (E_F) positions [21]. However, the corresponding bimetal nano-floating-gate does not show superior memory performance, and the synergistic effect of the binary system is unclear yet.

In this work, Ag and Pt NPs are self-assembled with a solution process to form a Ag–Pt bimetal nano-floating-gate, which results in a greatly enlarged memory window in the OFET memory compared with those using the corresponding monometal nano-floating-gate. Although there are more electrons and holes trapped into the Ag–Pt nano-floating-gate, the device exhibits excellent memory retention and endurance. The synergistic effect on the memory characteristics is attributed to the dipole enhancement induced E_F shifts in the blended Ag and Pt NPs, which possess different capping stabilizers and presumably opposite surface dipoles. This mechanism is supported by the electronic structure

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characterization, and it may offer a new strategy to improve the device performance of OFET nonvolatile memories.

2. Experimental

2.1. Material preparation

Pt NPs capped by polyvinylpyrrolidone (PVP, Sigma–Aldrich, M_W = 55,000 g/mol) were synthesized by a reported method [22]. Ag NPs capped by oleic acid and oleylamine (OA) were purchased from Suzhou ColdStones Tech and used as received. Polystyrene (PS) and 3-mercaptopropyl trimethoxysilane (MPTS) were purchased from Sigma–Aldrich. Pentacene was purchased from Tokyo Chemical Industry and pre-purified by vacuum sublimation. N-type heavily-doped Si wafers with 100-nm-thick SiO_2 on top were customized from Silicon Quest.

2.2. Device fabrication

The OFET memory structure is illustrated in Fig. 1, where the SiO_2/Si substrate acts as the gate contact covered by the control dielectric. The nano-floating-gate was prepared by a self-assembled solution process. After routine cleaning, the SiO_2/Si substrate was firstly exposed to MPTS vapor at 30 mbar for 12 h. The MPTS-treated surface was then immersed for 24 h in the solution containing Ag or Pt NPs, after which the substrate was thoroughly rinsed and dried. The role of MPTS is to immobilize a monolayer of the metal NPs on the substrate through covalent bonding, while physically adsorbed upper layers were removed by multiple rinsing [23]. To realize saturated adsorption of the metal NPs, the process was repeated four times under same conditions. For the Ag–Pt bimetal nano-floating-gate, the immersion in the Ag and Pt solutions was alternately performed for two cycles. Subsequently, a PS thin layer (~10 nm) was deposited by spin coating on the nano-floating-gate and plays a role of the tunneling dielectric [14]. After that, 40-nm-thick pentacene was deposited by vacuum sublimation at 0.2 Å/s on the PS surface in a high-vacuum evaporator (Kurt J. Lesker, $<10^{-6}$ mbar). Eventually, Cu drain and source contacts were fabricated by thermal evaporation through a shadow mask [24], which defines the channel length (L) and channel width (W) as 50 μm and 750 μm, respectively.

2.3. Device characterization

The surface morphologies of as-prepared nano-floating-gate were characterized with atomic force microscopy (AFM, Bruker Dimension Icon) in tapping mode. X-ray photoelectron spectroscopy (XPS, Kratos Axis Ultra, monochromatic Al $K\alpha$) was utilized to characterize the electronic structure of as-prepared nano-floating-gate on heavily-doped Si with only native SiO_2. The electrical characteristics of the OFET memories were carried out in dark at room temperature in a high-vacuum probe station (Lake Shore CRX-4K) connected to a semiconductor parameter analyzer (Keithley 4200).

3. Results and discussion

Fig. 2a–c shows the surface morphology of the nano-floating-gate, which demonstrate that both Ag and Pt NPs are well decorated on the MPTS-treated surface despite different capping stabilizers (OA/Ag-NP and PVP/Pt-NP). The metal NPs appear to be closely packed with NP sizes ranging from 10 to 20 nm. For the Ag–Pt nano-floating-gate, the Ag and Pt NPs are randomly blended, and the blending does not significantly modify the NP size and surface density. The estimated surface density of the

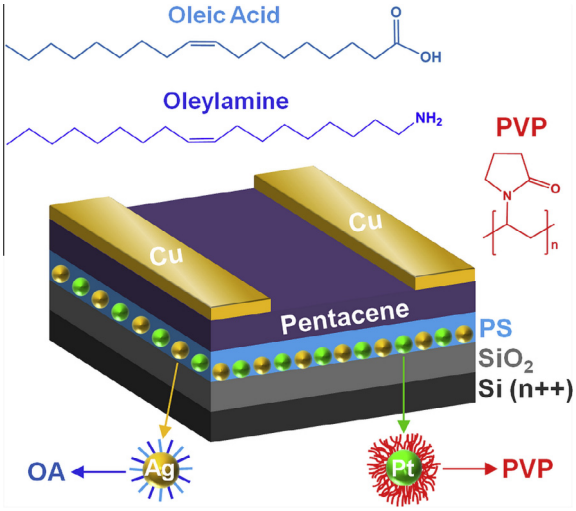

Fig. 1. Device structure of a pentacene-based OFET nonvolatile memory using Ag–Pt NPs as nano-floating-gate and PS thin layer as tunneling dielectric. Ag and Pt NPs are capped with OA and PVP, respectively, whose molecular structures are shown on the top.

Ag, Pt and blending NPs are about 3.1×10^{11}, 2.7×10^{11} and 2.9×10^{11}/cm^2, respectively. It is confirmed by the XPS spectra, which show the coexistence of Ag and Pt peaks with a full width at half maximum (FWHM) similar to that for the monometal nano-floating-gate. Upon the PS coating as shown in Fig. 2d–f, the PS surface is smooth and complete no matter on which nano-floating-gate. The total capacitances per surface area (C_i) of the dielectric layers including the nano-floating-gate are all about 30 nF/cm^2. The analogous PS layers and C_i allow a reliable comparison on the device behaviors of OFET memories based on different nano-floating-gate.

Utilizing the Ag, Pt or Ag–Pt blended NPs as the nano-floating-gate, the pentacene-based OFET memories were fabricated and their transfer characteristics are shown in Fig. 3a–c, respectively. The data marked with "initial, programmed and erased" correspond to the device states before programming/erasing, after programming at the gate bias (V_{GS}) of 45 V for 1 s, and after erasing at V_{GS} of −45 V for 1 s, respectively. During the transfer characteristics scanning, the drain bias (V_{DS}) is kept at relatively low bias of −3 V. To give a complete picture, Table 1 summarizes the following key parameters with errors of totally 15 devices: the FE mobility (μ_{FE}), initial V_T (V_{T0}), positive V_T shift after programming ($\Delta V_{T\text{-}p}$), negative V_T shift after erasing ($\Delta V_{T\text{-}n}$) and memory window ($\Delta V_{T\text{-}p} - \Delta V_{T\text{-}n}$). The OFETs show similar hole μ_{FE} of 0.5–0.6 cm^2/Vs which is typical for pentacene thin films, in accord with the analogy of the PS surfaces. In addition, the μ_{FE} values do not change after programming/erasing.

There are three important features in Fig. 3a–c: (1) Both $\Delta V_{T\text{-}p}$ and $\Delta V_{T\text{-}n}$, corresponding to electron and hole trapping into the nano-floating-gate, respectively, occur for all the OFET memories. Thus the Ag and Pt NPs can trap both holes and electrons, and it is reasonable considering a number of occupied and unoccupied states around E_F of the metal NPs. (2) $|\Delta V_{T\text{-}p}| < |\Delta V_{T\text{-}n}|$ is shown for the Ag-only device, indicating a preference of hole trapping in the Ag NPs. In contrast, $|\Delta V_{T\text{-}p}| > |\Delta V_{T\text{-}n}|$ is shown for the Pt-only device due to a preference of electron trapping in the Pt NPs. The different extent of ΔV_T are associated with the distinction in work function of Ag (~4.4 eV) and Pt (~5.6 eV) [21]. (3) Significantly, the Ag–Pt bimetal device shows surprisingly large $\Delta V_{T\text{-}p}$ and $\Delta V_{T\text{-}n}$, which result in a large memory window up to 18.7 V. Note that the memory window for the Ag–Pt device is much larger than