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Organic field-effect transistors based on single-crystalline active layer and top-gate insulator consistently fabricated by electrostatic spray deposition

Norio Onojima *, Shun Takahashi, Hiroki Saito

Interdisciplinary Graduate School of Medicine and Engineering, University of Yamanashi, Kofu 400-8511, Japan

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ABSTRACT

An electrostatic spray deposition (ESD) method was applied to prepare both crystalline domains of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) and insulating films of poly(methyl methacrylate) (PMMA) for fabricating top-gate single-crystal organic field-effect transistors (OFETs). The electrical characteristics of the top-gate device were compared to those of the bottom-gate one (SiO_2 bottom-gate insulator) with the same active layer, and the lower charge-trap density at the interface between the top-gate insulator and single-crystalline active layer was demonstrated. The drain current compression in the output characteristics of the top-gate device, however, occurred due to the large parasitic resistance between the source/drain electrodes and accumulation channel. Reducing the thickness of the single-crystalline active layer resulted in a high charge-carrier mobility of 0.29 cm^2/V s (channel length of 5 μm).

1. Introduction

Organic field-effect transistors (OFETs) fabricated by printing techniques have been expected to pave the way for low-cost and environmentally friendly electronics [1]. Specifically, high-speed OFETs have attracted much attention due to their potential application to logic circuits over large areas [2–6]. To improve high-frequency performance, the channel length (L) should be as short as possible since the switching speed is proportional to L^{-2}. In this regard, bottom-contact (BC) configuration has proven to be advantageous because fine photolithography can be applied to pattern the source/drain electrodes prior to depositing the active layer, and the channel length can be reduced to less than 10 μm [7]. The charge-carrier mobility (μ) between the source and drain electrodes is another important factor involved in the enhancement of high-frequency performance since the switching speed is proportional to μ. Charge transport takes place within the first several molecular layers at the interface between the gate insulator and active layer [8]. Therefore, the magnitude of μ is greatly affected by interface properties such as the charge-trap density [9]. Many Si-OH silanol groups exist on the surface of SiO_2, and they act as charge-trap sites when SiO_2 is used as a gate insulator. On the other hand, poly(methyl methacrylate) (PMMA) is more suitable for use in OFETs because it provides a trap-free interface due to the absence of hydroxyl groups [8].

In our previous work, we fabricated pentacene-based OFETs with PMMA top-gate insulators (channel length of 5 μm) prepared by electrostatic spray deposition (ESD) [10]. Top-gate devices have many advantages over bottom-gate ones. However, the charge-carrier mobility was as low as 4.6×10^{-2} cm^2/V s because the vacuum-evaporated pentacene active layer grew in polycrystalline state including many grain boundaries. To obtain a higher charge-carrier mobility, using a single-crystalline channel is more favorable because no domain boundaries are present between the source and drain electrodes [11,12]. We have also reported that large crystalline domains (a few hundred micrometers in size) of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) were prepared by ESD and used as single-crystalline channels in OFETs with SiO_2 bottom-gate insulators [13]. A charge-carrier mobility of 0.11 cm^2/V s was obtained in a bottom-gate single-crystal device with a channel length of 5 μm.

In the present work, the ESD method was applied to prepare both crystalline domains of TIPS pentacene and insulating films of PMMA for fabricating top-gate single-crystal OFETs, and a 5 μm channel length device with a charge-carrier mobility of 0.29 cm^2/V s was achieved. A simple and efficient roll-to-roll process can be achieved by applying a consistent printing technique for fabricating all the layers of an OFET.

* Corresponding author.
E-mail address: nonojima@yamanashi.ac.jp (N. Onojima).

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2. Experimental

A schematic of our ESD system and the device architectures fabricated in this study are illustrated in Fig. 1. ESD is a printing technique that enables us to deposit organic films selectively using a shadow mask. Compared to conventional spin coating process involving significant material waste, the ESD method has the advantage of high deposition efficiency as the droplets are transported by electrical forces. It is worth mentioning that using post-drying treatments with high curing temperature to evaporate residual solvents is not required owing to the intermediate process between dry and wet conditions. This feature is desirable since most organic films are very vulnerable to heat [14]. The most significant advantage of spray technology is related to its compatibility with industrial-scale roll-to-roll processes [15]. Fig. 1(a) depicts a bottom-gate structure after depositing an active layer using a TIPS pentacene solution, and Fig. 1(b) depicts a top-gate one after depositing a top-gate insulator using a PMMA solution. Heavily-doped n-type Si (100) substrates were used as bottom-gate electrodes (less than 0.02 Ω cm in resistivity). SiO_2 layers with a nominal thickness of 300 nm were thermally grown on the Si substrates and were used as bottom-gate insulators (12 nF/cm^2). 30-nm-thick Au source/drain electrodes with a Ni adhesion layer were patterned on the substrate via photolithography and lift-off processes. The channel length was 5 μm, and the channel width varied from 10 to 50 μm. The substrate patterned with BC electrodes was cleaned by soaking in conventional organic solvents (acetone, methanol, and ethanol) followed by UV/ozone treatment. A self-assembled monolayer (SAM) of pentafluorobenzenethiol (PFBT) was formed on the BC electrodes to modify the contact characteristics (30 min immersion in 5×10^{-2} mol/l PFBT solution with ethanol) [16]. A TIPS pentacene solution was sprayed onto the substrate in air at 50 °C. TIPS pentacene was dissolved in a mixed solvent of 1,2-diclorobenzene (o-DCB) and acetone (1:1 (v/v), 0.1 wt% in concentration). For multi-jet spraying (which is suitable for large-area uniform deposition) [17], it is necessary to mix the good solvent (o-DCB) with an additional solvent that has a high relative dielectric constant such as acetone (ε_r = 21.0) [18,19]. Details of the preparation condition of TIPS pentacene solution have been described elsewhere [13]. The ESD process that is closer to a wet condition is better to form larger crystalline domains than that is closer to a dry condition. The solution feed rate of 0.6–1.0 ml/min was precisely controlled by a syringe pump. The spraying time was 3 min. The spray-nozzle diameter, nozzle-substrate distance, and voltage applied to the nozzle were 250 μm, 5 cm, and 9–13 kV, respectively. PMMA top-gate insulators were deposited on the TIPS pentacene active layers at room temperature. PMMA was dissolved in a mixed solvent of butyl acetate and acetone (1:1 (v/v), 0.1 wt% in concentration). Details of the preparation condition of PMMA solution have been described elsewhere [10]. The solution feed rate, spraying time, spray-nozzle diameter, nozzle-substrate distance, and voltage applied to the nozzle were 0.066 ml/min, 45 min, 120 μm, 10 cm, and 10 kV, respectively. The PMMA film was prepared in an ESD process that is closer to a dry condition. To keep the dry condition, we used lower solution feed speed and smaller spray-nozzle diameter than those used in TIPS pentacene deposition. It should be noted that no drying treatment was carried out after depositing the PMMA top-gate insulators. Finally, 50-nm-thick Al was thermally evaporated onto the PMMA top-gate insulator through a shadow mask to define the top-gate electrodes. The relative dielectric constant of the PMMA film was measured using an HP 4284A Precision LCR meter and was evaluated to be 3.1. The electrical characteristics of OFETs were measured in ambient air using Keithley 2400 and 236 source/measure units.

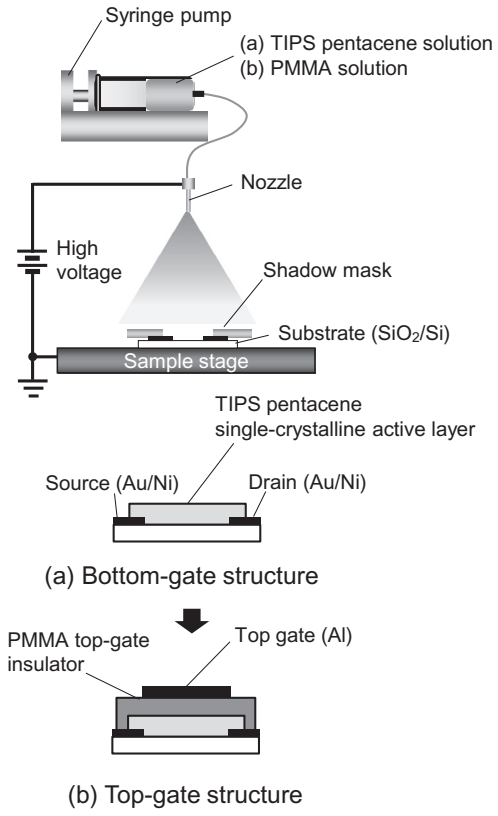

Fig. 1. Schematic of our ESD system and device architectures fabricated in this study: (a) after depositing TIPS pentacene active layer and (b) after depositing PMMA top-gate insulator.

3. Results and discussion

Fig. 2(a) shows an AFM image of the TIPS pentacene crystalline domain. A very smooth surface with monolayer steps can be observed. The root-mean-square (RMS) roughness was 2.3 nm over an area of 20 × 20 μm. On the other hand, the surface of the PMMA film was very rough (the RMS roughness of 117.9 nm over an area of 20 × 20 μm) (see Fig. 2(b)) because the PMMA film was prepared in an ESD process that is closer to a dry condition. In the dry condition, almost all of the solvents of PMMA droplets (butyl acetate and acetone) evaporate prior to arriving at the substrate, resulting in very rough morphology. It should be noted, however, that transistor behavior could not be achieved when the PMMA top-gate insulators were prepared in the ESD process that is closer to a wet condition because the residual solvents dissolved the underlying active layer [10]. From a SEM image of PMMA particles deposited on the SiO_2 (Fig. 2(c)), the size of the PMMA particles were found to range from 1 to 5 μm. Thus, the PMMA films prepared in the dry condition would be constituted by these particles.

The output characteristics of the bottom-gate (after PMMA deposition) and top-gate OFETs with the same active layer composed of a single-crystalline domain (800 nm in thickness) are shown in Fig. 3(a) and (b), respectively. Here, the thickness of the PMMA top-gate insulator was about 300 nm (300 ± 50 nm). The output characteristics were measured with a gate bias that varied from 0 to −50 V in steps of −10 V. The maximum drain currents (at a gate bias of −50 V) for the bottom-gate and top-gate devices were −94 and −180 μA/mm, respectively. Since the capacitance of the 300-nm-thick PMMA top-gate insulator was 9.1 nF/cm^2 (the value of the SiO_2 bottom-gate insulator was 12 nF/cm^2), this result