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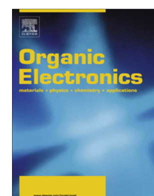

High-speed organic transistors with three-dimensional organic channels and organic rectifiers based on them operating above 20 MHz

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ABSTRACT

Three-dimensional organic transistors (3D-OFETs) comprising vertical short channels are developed to raise the operational speed of organic transistors. The devices with a short-channel length of 0.8 μm and reduced parasitic capacitance operate at up to 20 MHz with an applied drain voltage of −15 V. Organic rectifiers based on the diode-connected 3D-OFETs are also demonstrated to operate at above 20 MHz, even with an applied effective voltage of about 4 V, which is higher than the speed of radio frequency identification tags of 13.56 MHz required in near field communication. These techniques boost the performance of organic transistors and can help to realize the breakthrough for practical applications of organic logic circuits used as key components in various flexible or plastic devices.

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1. Introduction

Organic transistors have been an attractive candidate as key components for realizing flexible or wearable devices, which can be fabricated by simple processes on plastic substrates [1–3]. Recent development of high-mobility, reaching and exceeding 10 cm^2/V s [4–7], and thermally-stable organic semiconductor materials have raised the possibility of practical applications in industry. Some of the researches have been dedicated to the development of organic logic circuits [8–10]. In order to realize commercial devices, the operating speed must be reasonably high, because thousands of transistors should work at the same time. For example, a 64-bit shift-register to operate radio frequency identification (RFID) tags includes more than 2000 transistors, and each transistor should work much faster than the clock speed to drive the next-stage circuits, typically to be at least several MHz for one transistor to operate a whole circuit with a clock speed of several tens of kHz. Thus, short-channel and high-mobility transistors are strongly required, because the cut-off frequency f_c of a transistor is described as

$$f_c = \frac{\mu_{eff} V_D}{2\pi L^2}\left(\frac{c_i WL}{c_i WL + C_{para}}\right), \quad (1)$$

in the linear regime, while V_D is replaced by V_G in the saturation regime. μ_{eff} is the effective carrier mobility of an organic semiconductor including the effects of contact resistance, C_{para} is the gate parasitic capacitance, and $c_i WL$ represents the channel capacitance. Short-channel and high-mobility transistors are of great importance also in the aspect of the circuit density, as we can recognize the great advances in silicon technologies along with the down-sizing technique and integrated density of the circuits. We note that the ratio of the channel capacitance compared to the total gate capacitance is also a crucial

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factor to decide the operational speed of transistors. Gate parasitic capacitance is determined by the overlap area of a gate electrode and source/drain electrodes. In the case of a top-contact configuration, which is favorable to reduce the contact resistance easily, the overlap length must be long enough to secure effective carrier injections [11], which is a trade-off relation for reducing the gate parasitic capacitance. Thus far, many researches have been devoted to reduce the overlap length to the minimum to speed-up organic transistors [11].

We have previously proposed three-dimensional organic field-effect transistors (3D-OFETs) integrating vertical short-channels, in which the large drain current density and high operating speed were demonstrated [12,13]. Since their channel lengths are defined as the heights of the microstructures, even the short channels with sub-micrometer size can be fabricated using photolithography technique beyond the in-plane patterning resolution. In our previous reports, however, the operational speeds are limited to a several MHz by the large parasitic gate capacitance, though the sub-micrometer channels can be fabricated with a fair carrier mobility and the calculated frequency with no parasitic capacitance is reaching 100 MHz [13]. As one of the important applications of organic transistors, RFID tags used in near field communication should response at 13.56 MHz, therefore, an operating speed of at least a few tens of MHz is a highly meaningful technical target for organic transistors to be reached. In the present study, we have developed new 3D-OFET structures with patterned gate electrodes only in the vicinity of the sidewalls in order to reduce the parasitic gate capacitance drastically. The cut-off frequency of as high as 20 MHz is demonstrated with the fabricated devices and organic rectifiers based on the high-speed 3D-OFETs are substantiated operating at up to 20 MHz.

2. High-speed organic transistors based on 3D structures

2.1. Fabrication of 3D organic transistors with reduced gate capacitance

Fig. 1(a) shows a cross-section of a fabricated 3D-OFET with a patterned gate electrode. Organic semiconductor channels are built on the sidewalls of the micro-structures vertically on the substrate with a channel length of 0.8 μm. Since the channel length direction corresponds to the height direction of the structures, short-channel devices can be easily fabricated. Process flow to fabricate a 3D structure with a patterned gate is shown in Fig. 1(b): The micro-structures to build the 3D vertical channels were fabricated using a negative-tone photoresist SU8™ (Nippon Kayaku, Microchem Co., Ltd.) on EAGLE XG® (Corning Inc.) glass substrates. The height of the structures was defined to be 1.5 μm to form the device with the channel length of 0.8 μm, which is observed using scanning electron microscopic (SEM). After an aluminum film was vacuum-deposited to cover whole surfaces of the structure, a photoresist layer was formed and patterned using photolithography, leaving the photoresist only on the sidewalls of the structures. Then the aluminum gate film located on except the area of the sidewalls was wet-etched using the photoresist as a mask, and finally the photoresist film was removed to produce the patterned gate structures. Fig. 2(a) and (b) shows optical micrographs and scanning electron microscopic (SEM) views of the obtained structures with the patterned gate. We note that the gate film was successfully formed only on the part of the sidewalls on the structures. Parylene dix-SR® (KISCO Ltd.) was deposited as a gate insulator on this structures to the thickness of 120 nm, and dinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-b]thiophenes (DNTT) [14] was vacuum-

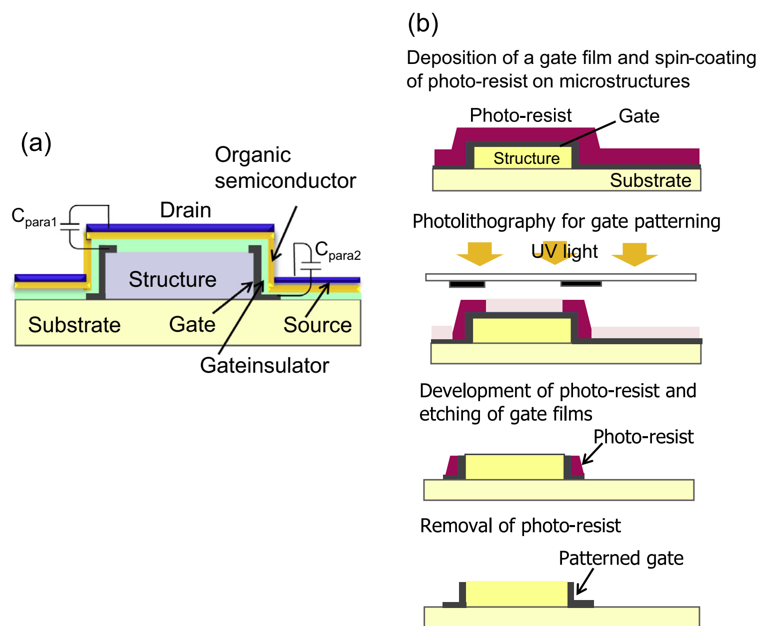

Fig. 1. (a) Cross-sectional view of the 3D-OFETs with reduced C_{para}. (b) Process flow to fabricate 3D structures with patterned gate electrodes.

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