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Fully-printed, all-polymer, bendable and highly transparent complementary logic circuits



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ABSTRACT

In this contribution we show a simple approach for the development of all-polymer based complementary logic circuits fabricated by printing on plastic, at low temperature and in ambient conditions. This is achieved by patterning, with a bottom-up approach, solely synthetic carbon-based materials, thus incorporating earth-abundant elements and enabling in perspective the recycling – a critical aspect for low-cost, disposable electronics. Though very simple, the approach leads to logic stages with a delay down to 30 µs, the shortest reported to date for all-polymer circuits, where each single component has been printed. Moreover, our circuits combine bendability and high transparency, favoring the adoption in several innovative applications for portable and wearable large-area electronics.

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1. Introduction

The field of flexible microelectronics, where bendable and even conformable substrates are adopted, has the appealing potentiality of facilitating the integration of electronic functionalities into innovative light-weight products. To this purpose, organic materials represent one of the most suitable candidates because of clear advantages such as their good mechanical flexibility and the chemical tunability of the opto-electronic properties, achieved by exploiting a vast library of molecules and functional groups. Furthermore, their solubility in organic solvents enables the use of printing and coating techniques, highly desirable in the context of large area and low-cost tech-

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http://dx.doi.org/10.1016/j.orgel.2015.02.006 1566-1199/© 2015 Elsevier B.V. All rights reserved. nologies [1,2]. Printing enables device mass-production requiring low capital investments, as well as highly customized applications at sustainable costs thanks to digital techniques, such as inkjet printing [3]. Polymer-based opto-electronic devices on plastic substrates, such as flexible displays [4], large-area chemical and physical sensors [5,6], and photodetectors [7,8] have been widely explored. Polymer logic gates and circuits are necessary to obtain fully-integrated systems, as they provide essential data computation and matrix addressing functionalities [9]. Recent progress in this area has led to field-effect transistors with impressive mobilities, greater than 1 and $10 \text{ cm}^2/\text{V}$ s for *n*- and *p*-type donor-acceptor co-polymers, respectively [10]. Thus, high performance electronic elements are at hand, since hole/electron mobilities are now a far less limiting aspect than it was only a few years ago.

However, major efforts are necessary to move the field from a single high-performance transistor to more complex circuits, essential for commercial applications [11]. Yet, most of transistor integration studies combine hybrid approaches. where besides the organic semiconductor, either the dielectric, the electrical contacts. and the substrate are fabricated by vapor deposition, or are mechanically rigid. These limitations, combined with the use of non-scalable techniques, undermine the whole printed electronics concept [12]. Transparency, or semitransparency, is also a highly demanded feature for flexible electronics as it would allow delivering active electronic circuits on top of labels or graphic illustrations. Furthermore, polymer electronics is one of the best candidates for cheap, short life-time cycle, disposable mass products. Therefore a reasonable question about the environmental impact of the supply of raw materials and of the dispersion of large quantity of plastic arises, imposing to develop earth-abundant and recyclable materials [13].

Reports combining all the requirements highlighted above are very rare in the literature, and usually comprise discrete, often very low performance, devices, which operate at frequencies well below the kHz regime. Here we address the challenge of fabricating robust, complementary logic circuits by adopting only scalable techniques in ambient conditions and at low temperatures (maximum processing temperature \sim 120 °C). These devices are based on well known model polymers such as poly([N,N'-bis(2octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene) (P(NDI2OD-T2)), as the electron-transporting polymer and diketopyrrolopyrrolethieno[3,2-b]thiophene copolymer (DPPT-TT) as the hole semiconductor. In the light of realizing fully carbon-based and highly transparent circuits, we used highly conductive formulations of poly(3,4-ethylenedioxythiophene): polystyrene sulfonate (PEDOT:PSS) for the electrodes. While efficient hole injection is expected through PEDOT:PSS, thanks to a suitable nominal matching of the highest occupied molecular orbitals (HOMO) of most high-performance semiconducting polymers, its use for complementary circuits is less obvious because of a nominally less favorable matching with the lowest occupied molecular orbitals (LUMO), which usually requires low work function electrodes. We show that optimal device performances are achievable in both cases for channels down to a few tens of micrometers, thanks to a surprisingly low contact resistance of 33 k Ω cm in the case of *n*-type devices. Such value is achieved without the need of an additional charge injection layer [14,15], thanks to interfacial effects reducing the nominal barrier for electron injection.

Regarding the deposition techniques of the functional materials, we employed ink-jet printing, which is a noncontact digital technique requiring minimum amount of inks [3] to pattern the electrodes and the semiconductors. Since inkjet printing is less suitable for fast uniform coatings, required e.g. for the dielectric and passivating layers, we have adopted bar-coating [16], a rugged coating technique which enables the fine control of film thickness over large areas.

Our approach is very simple, and it is compatible with the fabrication of complementary inverters and ring-oscillators and more complex circuits such as logic latches, i.e. dynamic storage elements. Thanks to the good mobility of the selected semiconductors and the optimal characteristics of the resulting devices, logic gates show stage delays down to 30 μ s, by far the shortest reported to date for truly all-printed, all-organic circuits on plastic substrates. Moreover, these circuits are highly transparent (>90% not considering the substrate) and flexible (no mobility degradation up to 1% of tensile strain). Thus, these results form a solid base for the further development of transparent, all-polymer circuits enabling complex logic functionalities to be integrated in future cost-effective, wearable, portable and ubiquitously integrated electronic devices.

2. Materials and methods

2.1. Materials

P(NDI2OD-T2) was purchased from Polyera and DPPT-TT was synthesized using the method explained by Chen et al. [17]. Poly(methyl methacrylate) (PMMA) was purchased from Sigma Aldrich (average $M_w \sim 120,000$). PEDOT:PSS formulations Clevios Pjet700 and Clevios PjetN were purchased from Heraeus, while Orgacon ICP1050 was purchased from Sigma Aldrich. The 125 µm thick poly (ethylene 2,6-naphthalate) (PEN) substrate was purchased from DuPont.

2.2. Device fabrication

We inkjet printed all the PEDOT:PSS formulations for conductivity characterization and source/drain/gate patterning by means of a Fujifilm Dimatix DMP2831. After printing, the PEDOT:PSS features were baked at 110 °C for 30 min. Both semiconductors were deposited by inkjet printing and subsequently baked: P(NDI2OD-T2) was dissolved in mesitylene with a concentration of 5 mg/ml and baked at 120 °C for 12 h; DPPT-TT was dissolved into mesitylene at a concentration of 5 mg/ml and baked at 120 °C for 12 h. PMMA was dissolved in anhydrous n-butyl acetate with a concentration of 80 mg/ml. Dielectric coating of the devices was performed through a custom barcoater with a 50 mm/s speed and a bar with a 12 μ m wire diameter. After deposition, PMMA film was annealed at 80 °C for 30 min. Finally, PEDOT:PSS (Pjet700) was inkjet printed to make the gate electrode and annealed at 110 °C for 30 min to remove the excess solvent. For circuits, via-holes interconnections were realized through chemical drilling by inkjet printing the solvent directly onto the PMMA surface and filling the holes with PEDOT:PSS.

2.3. Measurements

The work function of the three PEDOT:PSS formulations (Pjet700, PjetN and ICP1050), as well as the electronic structure at the interface with the *n*- and *p*-type semiconductors were evaluated by means of ultraviolet photoemission spectroscopy (UPS). More details on the preparation of the samples and on the experimental setup for the photoemission measurements are included in the Supplementary Information. The transparency of all-printed devices was

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