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Pulsed voltage driven organic field-effect transistors for high stability transient current measurements

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ABSTRACT

In this article, we propose the usage of gate voltage pulses of alternating polarity, to effectively suppress the hysteresis in organic field effect transistors (OFETs). The hysteretic behaviour of poly(3-hexylthiophene-2,5-diyl) (P3HT) based OFETs is systematically investigated by using continuous and pulsed sweep voltage mode. On the basis of the experimental results, both time settings and mode of gate bias voltage influence the carrier transport in the semiconductor channel. Hysteresis-free transfer characteristic curves are obtained by applying diametrically opposed gate pulses of a few milliseconds in duration. Stable on-current transient measurements are also achieved by implementing the pulse mode, thus allowing on-line gas sensing measurements to be successfully performed. Finally, the response of the sensor upon exposure to different concentrations of analyte vapours is found to be in good agreement with the Langmuir adsorption isotherm model.

1. Introduction

Organic field effect transistors (OFETs) have evolved remarkably during the last decade, covering a broad range of chemical- and bio- sensing applications [1–5] and being closer than ever to be commercialized as low cost, robust and flexible organic devices. OFET-based sensors offer: (a) multiparametric analysis [6], thus providing rich sensing information, and (b) signal amplification, due to gating that improves signal-to-noise ratio (S/N) and enhances sensitivity [7]. However, the main obstacles on the way to reach large scale industrial application are the short lifetime and instability under operation. Hysteretic behaviour between forward and reverse voltage sweep and misleading threshold shifts due to biasing stress, are two features that reveal the poor stability in the performance of an OFET device [8–10]. In several cases, threshold voltage is recorded as the output signal of the sensor, and the V_{Th} shift is correlated with the sensing mechanism. But what happens if the V_{Th} shift is of the same order as the hysteresis width? Such an effect queries the reliability of the sensor. Trapping of charges or charge injection phenomena can occur, and possibly cause a threshold shift and drain current losses. The appearance of such undesirable defects in transistors operation can be due to several issues, such as: the nature of the involved materials (i.e. semiconductor, gate dielectric and metal contacts), the fabrication process itself, the configuration layout, environmental conditions and, finally, the sweep range and duration of the applied voltages.

In order to obtain hysteresis-free and stable under stress bias OFETs, different methods have been suggested, depending on the mechanism from which hysteresis can be originated. A lot of research groups are focused on synthesizing semiconducting materials, that are stable against oxidation in ambient conditions [11–14]. In the case of solution processed organic semiconductor (OS), the solvent

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selection is also critical and can minimize the appearance of hysteresis. An appropriate choice of solvent with respect to the OS is expected to improve the performance of the device [15]. Hysteresis and bias stress instability have been associated with the presence of moisture in the organic semiconductor, or at the interface with the gate dielectric, particularly in the case of a SiO_2 or polar polymer dielectrics [8]. Modification of the dielectric surface using self-assembled monolayers (SAMs), or selection of hydrophobic dielectrics can decrease hysteresis. Hysteresis effects have been reduced by carefully selecting the gate dielectric in order to exhibit high dielectric strength, low leakage current, and high breakdown strength [9]. Moreover, the gate dielectric influences the hysteretic behaviour of OFETs, even if it is not directly involved in charge trapping. The polarity of the gate dielectric influences the electronic structure and density of states (DOS) of the organic semiconductor at the interface [16,17]. Charge injection from the gate electrode into the dielectric layer has been also found to be responsible for large hysteresis, especially in polymeric dielectrics. Deposition of inorganic-barrier layers in contact with the gate electrode has been also reported as a sufficiently performing solution to avoid hysteresis appearance [18]. Nevertheless, a complete encapsulation of the transistor is expected to improve the overall stability of the device under operation in ambient environment.

Herein, a pulse measurement method using voltages of alternating polarity (AP) is employed to reduce hysteresis in P3HT based OFETs transfer characteristics. A similar approach was indeed proposed for the first time some years ago [19]. AP pulse mode sweeps the gate voltage from negative to positive values (or vice versa), thus allowing the charges trapped by the negative pulse to be immediately detrapped by the positive one. In this way, an "intrinsic" transistor response with negligible charge-trapping effect can be measured. Compared to all the above listed approaches of reducing hysteresis, the pulse mode can be applied to all types of FETs regardless of the configuration and materials involved in the fabrication. We find that by varying the pulse-on and pulse-off time of the applied gate voltage, the current's forward and reverse curves coincide and lead to a single value of mobility. We adopt the same approach to evaluate the transistor's stability under operation by recording the drain current (I_{DS}) as a function of time, applying continuous and pulsed gate voltages. Furthermore, a comparison of the sensing performance of the OFET upon exposure to analyte vapours when it is operated in time under continuous and pulsed mode is also presented.

2. Materials and methods

In this study, OFETs bearing a bottom-gate/top-contact configuration (BGTC) were prepared according to the structure reported in Fig. 1a. Silicon wafers n-doped (n-Si) were used as substrates, featuring a thermally grown 300-nm thick silicon oxide (SiO_2) dielectric layer. The capacitance of the dielectric was 9×10^{-9} F/cm^2. At first, the substrates were rinsed with water/acetone/water, then

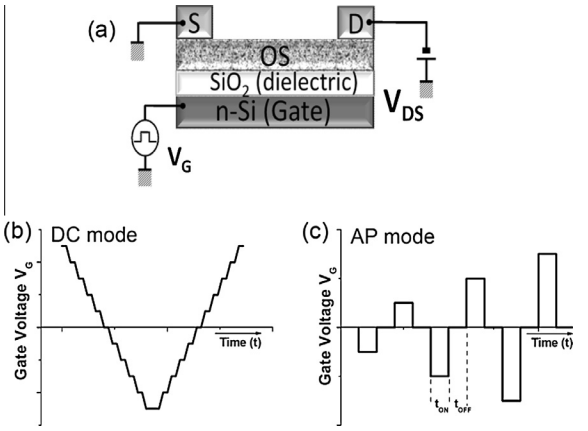

Fig. 1. (a) Schematic illustration of the BGTC OFET device. Gate voltage sweep (b) DC mode, and (c) AP mode.

dipped in an isopropanol ultrasonic bath for 15 min and dried under nitrogen (N_2) stream. The organic semiconductor is a commercial poly(3-hexylthiophene-2,5-diyl)—P3HT, regioregular, purchased from Rieke Metals, Inc. After purification, P3HT was dissolved in chloroform (2.5 mg/mL) and was spin coated at 2000 rpm for 60 s at room temperature. Source (S), drain (D) contacts were defined by thermal evaporation (10^{-6} Torr) of gold through a shadow mask. The obtained OFET devices had a channel length of 200 μm and a width of $W = 4$ mm. The doped bulk of the silicon wafers was used as the gate electrode. In order to contact it, part of the insulating thermal oxide layer was scraped off using a diamond tip. All the reagents, solvents included, were purchased from Aldrich and used without further purification.

Electrical measurements were carried out using a Keithley Model 4200-SCS semiconductor analyser. The drain to source transfer current (I_{DS}) curve was measured at different gate voltages (V_G) and at a constant source and drain bias (V_{DS}). The gate voltage was cycled from the OFF to the ON state and backwards in two different modes: (a) continuous mode (or normal DC sweep mode), and (b) pulsed mode of alternating polarities (AP sweep mode). In the continuous mode, the V_G is linearly swept (staircase type), while the current is monitored at each sweep step, as shown in Fig. 1b. The gate voltage is swept from +100 V to −100 V and backwards, with a step of 4 V at constant $V_{DS} = -80$ V. The double sweep is performed at three scan rates: 18 V/s (long), 20 V/s (medium) and 27 V/s (short). AP pulsed I_{DS}–V_G measurements were carried out by applying gate voltage pulse of a certain polarity (positive or negative) followed by a pulse of the same duration and amplitude but of opposite polarity from the previous, as can be seen in Fig. 1c. The gate voltage pulses were generated by selecting the voltage list sweep option, in the software provided by Keithley. The pulse amplitude was set to gradually increase from 0 to 100 V with a step of 10 V and backwards, while alternating the polarity at each step. Moreover, the Keithley 4200 SC offers the ability to set the desired pulse on and off time when selecting the pulse mode. Measurements were performed by varying