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Flexible organic transistors on standard printing paper and memory properties induced by floated gate electrode

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ABSTRACT

Integrating electronic devices with unconventional substrate has been a popular research direction. Among these substrates, cellulose fiber paper has advantages in low-cost, recyclable and bio-degradable. We demonstrated directing printing of all contact electrodes on standard untreated Fuji Xerox printer paper without using planarization layer. The screen-printed gate electrodes based on silver nanoparticles can smooth out the paper substrate surface by two orders of magnitude and allow us to use parylene and DNTT as the dielectric and active layer directly. The transistors show average mobility of 0.297 $cm^2 V^{-1} s^{-1}$ and on/off ratio larger than 10^5. The low leakage current allows us to demonstrate memory properties by employing the floated gate method. The devices show excellent memory retention time for more than 10,000 s. The unique flexibility and combustibility of the organic transistors on paper substrate manifest their applications as next generation of green electronics.

1. Introduction

Thanks to its mechanical flexibility, potentials in large-area and low-cost production, research on organic thin film transistors (OTFTs) has shown rapid development in carrier mobility, on/off ratio, device size, and substrates [1–4]. To date, flexible OTFTs are usually fabricated on common plastic substrates, such as polyimide (PI), poly(ethylenenaphthalate) (PEN) and poly(ethyleneteraphthalate) (PET) due to their reasonably good bending stability and relatively low surface roughness [5–7]. Recently, fabricating organic devices on unconventional substrates to explore new application potentials has gained a lot of attention, especially on paper substrates based on cellulose fiber. Organic photovoltaic cells and thin film transistors have been successfully demonstrated on paper substrates [8–14]. Comparing with polymer plastic substrates, papers have excellent flexibility, folding properties, chemical dissolvability, and higher tolerance in thermal annealing. Furthermore, the cost of paper substrates is extremely low (~\$0.001 dm^{-2}, FujiXerox) compared with silicon (~\$25 dm^{-2}, SiliconQuest) or polymer substrates (~\$1–10 dm^{-2}, Goodfellow). More importantly, the solar cells or transistors with paper substrates can be easily disposed by incineration or dissolved by biomaterials [15] or ionic liquid [16] without causing pollution problems. However, similar to other plastic flexible substrates, the roughness of the paper is critical to the growth mode of the organic semiconductors by thermal evaporation. Organic active layers deposited on rough surface with poor crystallinity will lower the effective carrier transport mobility and increase the leakage current of the OTFTs [17–19]. The roughness of these commonly used PI, PEN or PET substrates are usually in the magnitude of a few nanometers [20,21]. For extremely high performance devices or circuits, planarization layer is needed to reduce the roughness to sub-nanometer scale and comparable with Si/SiO_2 substrate. For example Someya et al., have employed

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500 nm of polyimide cured at 180 °C to reduce the roughness of 12.5 μm thick plastic substrate from 5 nm to 0.3 nm [7]. For rougher surfaces such as fabrics, artificial skins, or standard papers, a much thicker planarization layer is needed to smooth out the substrate roughness, which would also increase the complexity of device fabrication at the same time.

To overcome the large surface roughness issue, Alshareef et al. have used polymer planarization layer formed by 40 μm thick polydimethylsiloxane (PDMS) on banknote substrates for high performance OTFT memory devices with ferroelectric layer [10]. However, the thick PDMS layer may limit the flexibility of the paper substrates and may be challenging for large area fabrication. Also working on banknote substrates, Zschieschang et al. utilized thermal evaporated Al gate electrode with AlO_x and *n*-octadecylphosphonic acid (ODPA) self-assembled monolayer (SAM) dielectric to fabricate high performance OTFTs and inverters on banknote substrates [13]. Fortunato et al. have also nicely reported using hydrophobic paper as the substrate and dielectric layer for the complementary inverter with inorganic semiconductors gallium indium zinc oxide and tin oxide as channel materials [14]. Under similar structure with the paper substrate as the dielectric, Martins et al. successfully demonstrated paper based inorganic memory transistor with a long retention time [22,23]. The long charge retention time is due to the ultra stable traps state in the paper dielectric.

Here, we demonstrate direct printing of gate electrodes on standard printing paper (Fuji Xerox Business+) for transistor array fabrication without planarization layer or solution processed SAMs. The screen-printed silver gate electrodes can significantly reduce the average roughness (R_a) of similar paper substrates from 7 μm ([24] measured in 3 mm × 3 mm area) to 96 nm (measured in 10 μm × 10 μm area). By using a para-chloro-xylylene (parylene-C) dielectric layer and screen-printed source/drain electrodes, the dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) transistors show an average carrier mobility of 0.297 $cm^2 V^{-1} s^{-1}$ and average on/off ratio of 8.7×10^5 on the untreated Fuji Xerox paper. To the best of our knowledge, this is the first time organic electronic devices have been fabricated on conventional untreated paper substrate without using a planarization layer or SAM. The screen-printed gate electrodes play an important role in suppressing the surface roughness of the substrate and the averaged leakage current of the device is around 10 pA. The use of vapor deposition of dielectric and DNTT can eliminate the solvent absorption of the paper substrate during normal solution processing methods. We also study the memory properties of the novel OTFTs on paper substrates by floating the gate electrode during bias. The long lasting memory property of the transistor array after 24 h of storage indicates the potential applications of these devices in anti-counterfeiting or using as the real-time sensors. The current paper based OTFTs with all screen-printed electrodes do not require thermal evaporation, sputtering, solution processing or thermal annealing. It is an important step towards printing of large-area, low-cost, decomposable devices on standard cellulose fiber paper for green electronic applications.

2. Experimental

2.1. Device fabrication

99.95% pure nitrogen was used to blow away large dust on the Fuji Xerox printing paper (Fuji Xerox Business+, 80 gsm, 107 μm thick) before fabrication. Screen-printing process was completed by a home-made screen-printing system equipped with CCD cameras and manual XYZ-rotation stage for precise alignment (Fig. S1). Silver paste (RAFS 089, TOYOCHEM) was patterned by a screen mesh (ELECHEM TECHNOLOGY) with a printing speed of 5 cm s^{-1}. After the gate printing process, the Silver paste was dried in ambient air for 2 h. Parylene-C (J&K Scientific) was deposited onto the printed electrodes in a CVD system (Labcoater PDS 2010, Specialty Coating Systems). After that, 50 nm DNTT (Lumtec, Taiwan) was thermally evaporated on the parylene-C layer in an evaporation chamber (MiniBox Conversion, MOORFIELD) at a base pressure of 8×10^{-7} Torr. For the first 5 nm of DNTT, evaporation speed was controlled at 0.1–0.3 Å s^{-1}, and the rest 45 nm of DNTT was evaporated at 0.5–1.0 Å s^{-1}. DNTT was patterned by a PEN shadow mask cut by a CO_2 laser (VLS 2.30, Universal laser systems). The device is finished by screen-printing the top source and drain electrodes, followed by another 2 h drying process. After the whole fabrication process, the device was loaded into glove box (M-Braun) for electrical characterizations and storage.

2.2. Characterizations

Thickness of printed electrode is estimated by scanning electronic microscopes (Hitachi S-4800 FEG SEM, LEO 1530 FEG SEM). Surface roughness of printed electrode is determined by tapping mode of an atomic force microscope (Bruker NanoScope 8). Thickness of parylene is measured by a stylus profiler (P10, KLA Tencor). Capacitance measurement is done by an Agilent 4294A precision impedance analyzer. Electrical measurement of transistor is completed by 2 Keithly 2400 sourcemeters or a Keithly 2636A dual-channel sourcemeter. All the electrical tests, except the current measurements during bending test, are performed in glove box under dark with water and oxygen content less than 1 ppm. For the bending test, after certain bending cycles, the device was released to 0 strain and measured current in ambient air under normal laboratory illumination.

3. Results and discussion

3.1. Transistor on Fuji Xerox paper

The schematic drawing of the OTFT structure is shown in Fig. 1e. Twenty-five devices are fabricated on the paper substrate with an area of 6.45 cm^2 (1 in. × 1 in.). The silver paste is a blend of organic solvents and silver nanoparticles with average diameter of ~300 nm. High silver content in the paste (>80%) allows the printed electrodes to reach a volume resistivity of 10^{-4} Ω cm (60 times of bulk silver's volume resistivity) after drying for 1 h under ambient air