Organic Electronics 38 (2016) 186–192

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

All ink-jet printed low-voltage organic field-effect transistors on flexible substrate

Linrun Feng [a, 1, 2], Chen Jiang [b, 2], Hanbin Ma [b], Xiaojun Guo [a, *], Arokia Nathan [b, **]

[a] National Engineering Lab for TFT-LCD Materials and Technologies, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, 200240, People's Republic of China

[b] Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge, CB3 0FA, United Kingdom

ARTICLE INFO

Article history:
Received 4 July 2016
Received in revised form
4 August 2016
Accepted 21 August 2016

Keywords:
Organic field effect transistors (OFETs)
All ink-jet printed TFTs
Low-voltage operation

ABSTRACT

In this work, all ink-jet printed (IJP) low-voltage organic field-effect transistors (OFETs) on flexible substrate are reported. The OFETs use IJP silver (Ag) for source/drain/gate electrodes, poly(4-vinylphenol) (PVP) for gate dielectric, 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) blended with polystyrene (PS) as the semiconducting layer and CYTOP for encapsulation layer. All the printing processes were carried out in ambient air environment using a single laboratory ink-jet printer Dimatix DMP-2831. The all IJP device presents state-of-the-art performance with low operation voltage down to 3 V, small subthreshold swing (*SS*) of 0.155 V/decade, mobility of 0.26 $cm^2 V^{-1}s^{-1}$, threshold voltage (V_{th}) of −0.17 V and on/off ratio of 3.1×10^5, along with a yield of 62.5%. Through interface engineering and proper process optimization, this work demonstrates a promising low-voltage all IJP device platform for low-cost flexible printed electronics.

1. Introduction

Solution processed organic field-effect transistors (OFETs) have received considerable attention, owing to their attractive features of low-cost printable processes [1,2], superior intrinsic mechanical flexibility [3], and sustainable performance improvement [4]. These fascinating features of OFETs make them perfect candidates for applications as sensors [5], radio frequency identification (RFID) tags [6], smart memories [7], point-of-care diagnostic systems [8], flexible display backplanes [9] and wearable systems [10]. In the past few decades, apart from developing high mobility organic semiconductors [11], significant efforts focused on developing low-cost solution-based processes for OFETs [12–14], with ink-jet printing as one of the most promising candidates. Its merits include drop-on-demand direct patterning, non-contact mode, material saving and good compatibility with large area flexible substrates [15], all of which are highly desirable for low-cost and high-throughput electronics [16–19]. To further reduce the cost and improve the efficiency for OFETs' manufacturing, an all ink-jet printed (IJP) OFET device platform is highly very much in demand. Up to now, there have been very few publications on all IJP-OFETs [20–23]. Most demonstrate high operating voltage of typically a few tens of volts, which would be a bottleneck for most mobile or wearable applications where the electronics have to be powered with battery or AC field. Therefore, reducing the operating voltage of all IJP-OFETs has become a key challenge.

To reduce the operating voltage, we can increase the gate dielectric capacitance per unit area (C_i) [24] and/or reduce the semiconductor/dielectric interface trap density (N_{SS}) [25]. The larger C_i can be achieved by ultrathin or high-*k* gate dielectric. However, a thin gate dielectric can result in large gate leakage and a high-*k* gate dielectric would suffer from the interface dipole disorder [26], neither of which are compatible in all IJP-OFETs. For an all IJP-OFET, a bottom-gate bottom-contact (BGBC) device architecture is preferred [20–23], which prints source/drain electrodes on the dielectric layer rather than the process-sensitive semiconductor layer. In previous work, it has been shown that a reduced N_{SS} can be achieved with BGBC device architecture by using a blend of small molecule organic semiconductor and polymer binder [25,27–30]. Such an approach would be more compatible with ink-jet printing processes, which provides more flexibility on the

* Corresponding author.
** Corresponding author.
E-mail addresses: x.guo@sjtu.edu.cn (X. Guo), an299@cam.ac.uk (A. Nathan).
[1] Visiting with Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, United Kingdom.
[2] Linrun Feng and Chen Jiang contributed equally to this work.

http://dx.doi.org/10.1016/j.orgel.2016.08.019
1566-1199/

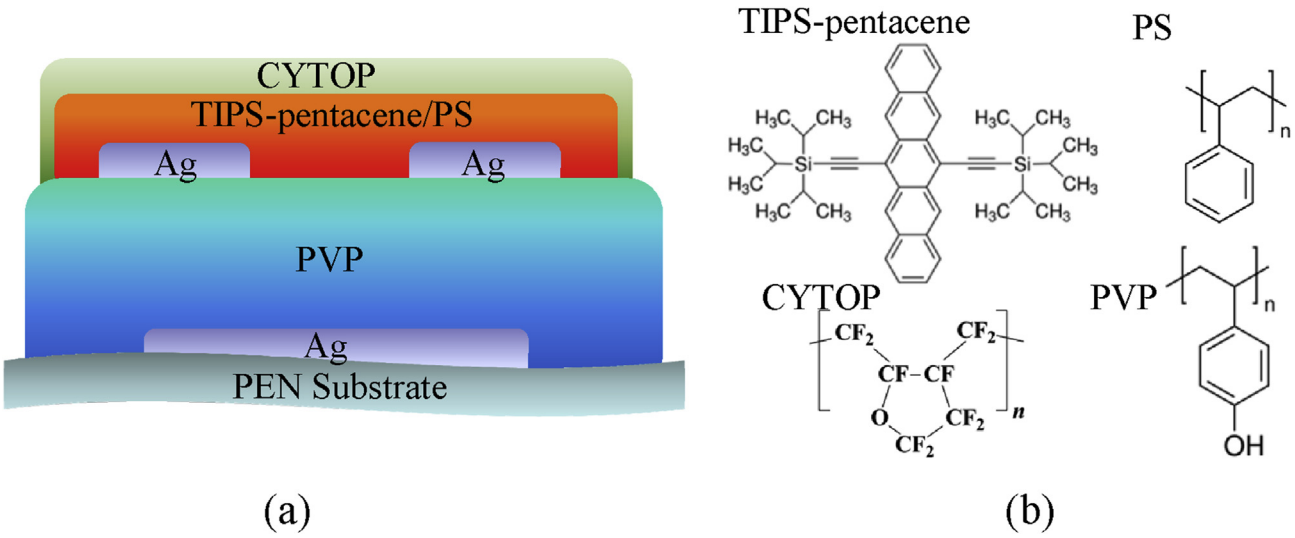

Fig. 1. (a) Schematic diagram of the all IJP-OFETs. (b) Chemical structure of the used materials.

dielectric thickness and dielectric constant (k) of the gate insulator. In addition, a higher mobility of IJP TIPS-pentacene OFET can be also achieved by blending with insulating polymer [31].

In this work, we adopt the approach of reducing N_{SS} and show that it is effective. Based on a small molecule organic semiconductor blended with polymer dielectric material system, combining with careful process optimization, a low-voltage (<3 V) all IJP-OFETs on flexible polyethylene naphthalate (PEN) substrate is reported. This work shows the first time through interface engineering and proper process optimization, all IJP low-voltage OFETs on flexible substrate can be achieved in ambient air lab environment.

2. Experimental

The device structure of the all IJP-OFETs and the chemical structure of the used materials are shown in Fig. 1(a) and (b), respectively. The BGBC devices were fabricated on a 125-μm-thick PEN substrate from DuPont. The size of the PEN was 4 cm × 4 cm. The Ag ink (jet-600C) was supplied by Hisense Electronics, Kunshan, China, and the CYTOP (CTL-809M) and its solvent (CT-Solv. 180) were provided by Asahi Glass. All other chemicals were purchased from Sigma-Aldrich. The poly(4-vinylphenol) (PVP) was dissolved in propylene glycol monomethyl ether acetate (PGMEA) at a concentration of 80 mg/mL. Subsequently, the cross-linking reagent poly(melamine-*co*-formaldehyde) (PMF) was mixed into the solution at a mass ratio of 1:2 to PVP. The mixed solution was then used as ink for the dielectric layer. We used a cross-linkable PVP dielectric as it has been proven to be a suitable gate dielectric for ink-jet printing process, and frequently used in the all IJP-OFETs [20–23]. The ink of semiconductor layer was prepared by mixing 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-

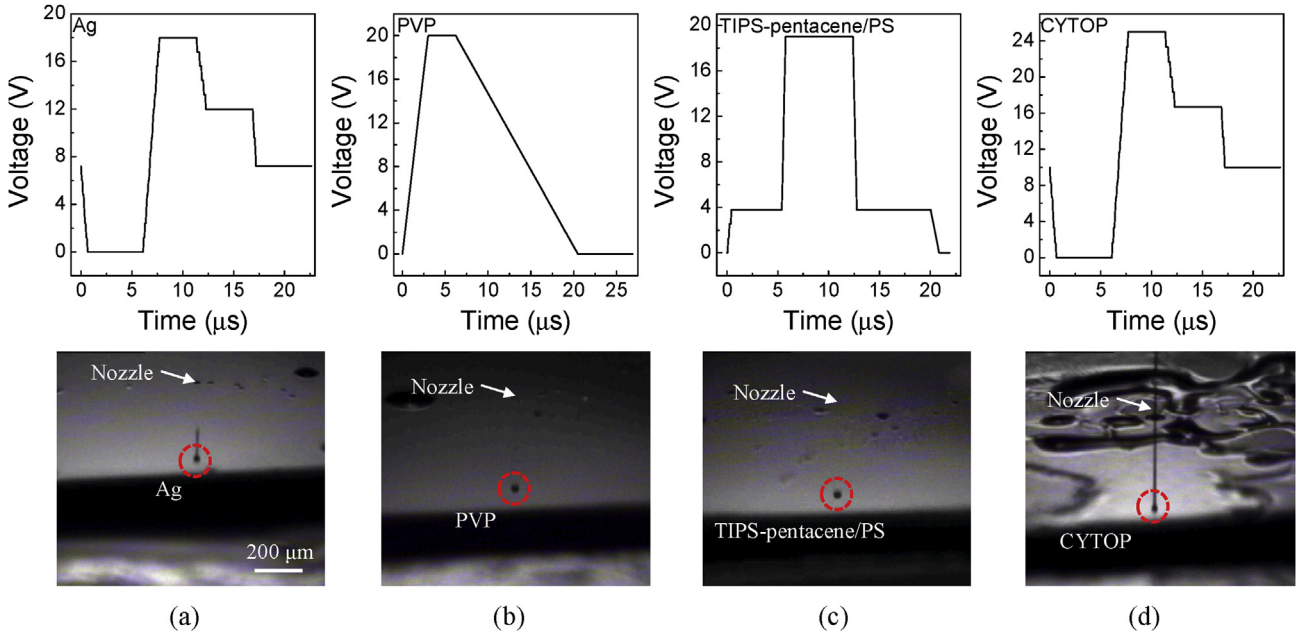

Fig. 2. Controlling voltage waveform for the ink-jet printing process and photograph of the ink-jetted drops from nozzle for (a) Ag, (b) PVP, (c) TIPS-pentacene/PS and (d) CYTOP.