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Organic field-effect transistors with cross-linked high-*k* cyanoethylated pullulan polymer as a gate insulator

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ABSTRACT

Low-voltage operable organic field-effect transistors (OFETs) were fabricated with a high-*k* polymer gate insulator, consisting of cyanoethylated pullulan (CEP) and poly(methylated melamine-co-formaldehyde) (PMMF) as a cross-linker. Effect of the cross-linker amount on the dielectric properties of the film was studied and transistor performance was evaluated. At the optimum PMMF contents, field-effect mobility as high as 2.16 cm^2/V s, on/off current ratio of $\sim 3 \times 10^5$, low hysteresis ($\Delta V_{th} \sim 0.01$ V) and a steep inverse subthreshold slope of 0.066 V/dec were obtained. A utilization of stainless steel as a gate metal and substrate markedly improved the device performance under a low-voltage operation ($\sim$1 V) due to the positively shifted threshold voltage from the work function change. The devices showed very little degradation in electrical properties with bending.

1. Introduction

Over recent years, there has been a great deal of research effort on organic field-effect transistors (OFETs) for their use in ubiquitous and low cost flexible electronics [1–3]. Mobility (μ) of OFETs with pentacene active layer has already been improved to a level comparable with amorphous hydrogenated silicon (a-Si:H) [4]. On the other hand, utilization of a polymeric gate insulator is likely to be an important step in developing all-organic transistor [5] and flexible electronics [6]. However, challenges for realizing practical applications remain such as developing a polymeric gate dielectric with high dielectric constant, low charge trap density, and mechanical robustness for low-voltage operable, low hysteresis and flexible OFETs [7].

Conventional thin-film transistors require high operating voltages (>20 V) and thus lead to the problem of high power consumption. There are a number of potential electronic applications that demand moderate computing power and low price for portable applications, such as electronic papers and radio frequency identification (RFID) tags [8,9]. Low-voltage operation can be achieved by using high capacitance dielectrics, which are typically high-*k* or ultra-thin films [3,8,10–12]. Efforts have been made on utilizing self-assembly monolayer (SAM) [9,13], multilayer [14], high-*k* inorganic/smooth organic bilayer structures [15,16], polymer electrolytes, and ion gels [17,18]. However, pathways for integration of SAM into large-volume coating processes are less obvious [19], and fabrication of inorganic part in bilayer structures always requires high vacuum, high temperature steps and sacrifice in flexibility. Therefore, a single organic dielectric layer is desired to allow a cost effective simple solution process at low temperatures [20].

Another issue in OFETs is electrical instabilities such as hysteresis that should be minimized from the viewpoint of reliability in practical applications [7,21]. There are several arguments as to the mechanism of the electrical instabilities in OFETs with a polymeric gate insulator [22]. A hysteresis loop can show a clockwise or an anti-clockwise direction with the change of the sweeping voltage, which can be referred to as clockwise hysteresis and anti-clockwise hysteresis. An anti-clockwise hysteresis generally occurs

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when an inorganic gate insulator is applied. For example, it was observed in the pentacene/SiO_2 interface where hydroxyl (OH) group was proved to provide electron traps [23]. Ambient moisture diffusion into the interface between the pentacene and the gate dielectric [24] layer along with impurities, defects as well as grain boundaries in semiconductor [25,26] also act as charge traps. A clockwise hysteresis is also associated with a polymeric gate insulator, and is often induced by the charge injection from the gate electrode and trapping inside the dielectric [27]. The dielectric bulk trapped electrons induce more holes in the channel and result in larger drain current during the bias sweep loop, contributing to clockwise hysteresis [28]. Lee et al. added SiO_2 buffer layer in between polymer insulator and gate electrode and proved the evidence of the electron injection from the gate electrode into the dielectric [21]. Additionally, residual dipole or mobile ions cause slow polarization in the bulk of the organic dielectric. The dipole reorientation process makes the drain current fall behind the bias sweep and a clockwise hysteresis appears [29]. Under a negative gate bias, migration of ions from internal impurities in polymer can also induce a similar effect [30].

Another advantage of the polymeric insulator is its flexibility [6] and flexible OFETs have been reported by many groups on a polymer substrate such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN) with a conductive organic electrode (PEDOT:PSS) and a polymer insulator (PVP, PVA, PS) [31–33]. On the other hand, stainless steel substrate is one of the flexible substrates with high corrosion resistance, high conductivity and thermal stability [34,35]. Its excellent thermal conductivity as a metal is helpful for the thermal management of the organic device. Through chemical mechanical polishing (CMP) process, a stainless steel substrate can have smooth enough surface to serve as a gate electrode [36].

In this report, OFETs were fabricated using a cross-linkable high-*k* CEP/PMMF blend with various mixing ratios as a dielectric to achieve OFETs with low voltage, low hysteresis operation with high μ and steep inverse subthreshold slope (SS). Stainless steel substrate was studied as a gate electrode and as a substrate to fabricate flexible devices. Electrical performance of OFETs on N+Si and stainless steel were also compared and bending effect on the device performance was studied.

2. Experimental

Fig. 1a and b shows the molecular structure of CEP (cyanoethylated pullulan) and PMMF [poly(methylated melamine-co-formaldehyde)] and the structure after cross-linking. Fig. 1c shows the schematic of MIM (metal–insulator–metal) structure, MIS (metal–insulator–semiconductor) capacitor and a top-contact pentacene OFET. The cross-linkable solution was prepared in a co-solvent (*N*,*N*′-dimethylformamide:acetonitrile 1:1) with 5 wt.% CEP ($M_w \sim 489{,}000$, Shin Etsu Chemical Co.) and various amount of PMMF (Aldrich, $M_n \sim 511$). PMMF/CEP ratios were set at 10%, 30%, 50%, and 70% to study the effect of the cross-linker content on the film properties and device performances. The solid films were formed with spin coating on piranha cleaned p-type (for MIS capacitors) or heavily doped n-type (for MIM structures and OFETs) silicon wafers at 3000 rpm for 1 min inside the high purity Ar-filled glove box. The film was annealed for 1 h inside a vacuum oven at 200 °C. The baked films were referred to as CEPM10, CEPM30, CEPM50 and CEPM70 for each PMMF content. After forming the dielectric, a 60 nm thick pentacene active layer (Aldrich Chemical Co., without purification) was deposited in a thermal evaporator with a deposition rate of 0.2–0.3 Å/s at a substrate temperature of 50 °C. Then 70 nm thick Au source and drain electrodes were deposited through a shadow mask, using the thermal evaporator; the device channel length and width are 150 and 1500 μm, respectively. For MIM structures and MIS capacitors, Au top (or bottom) electrodes were deposited with evaporation through a shadow mask to make a circular dot area of 8.02×10^{-4} cm^2.

Fourier Transform Infrared (FT-IR) spectra of solid films were recorded in a transmission mode with Nicolet 6700. Contact angle measurements were conducted using Model CA-A face contact angle meter (Kyowa Kaimenkagaku Co., Ltd.). Ultraviolet photoelectron spectroscopy (UPS) was used to calculate the work functions of the gate electrodes. The thickness of CEPM films were measured by ellipsometry. Capacitance–voltage (*C*–*V*) characteristics of the MIS capacitors were measured using HP 4284A Precision LCR meter (Agilent Tech.) at 1 MHz. The electrical characteristics of the pentacene FETs were measured using HP 5270A (Agilent Tech.) in a dark box under ambient conditions. To study the roughness of the dielectric surfaces, as well as pentacene morphology, atomic force microscopy (AFM) was adopted using a Dimension™ 3100 microscope (Digital Instruments). The in-plane X-ray diffraction (XRD) was carried out at the 3C2 X-ray scattering beamline of the Pohang Light Sources (PLS) at Pohang Accelerator Laboratory (PAL).

3. Results and discussion

3.1. Properties of CEPM and pentacene films

FT-IR spectra of the solid film in Fig. 2 were recorded in a transmission mode to monitor the chemical changes in the cross-linking reaction as demonstrated in Fig. 1b. The observed band between 3100 and 2800 cm^{-1} was assigned to the C–H (CH_x) stretching vibrations. As the PMMF content increased, slightly thicker film was obtained from higher material concentration, giving more intense CH_x peak. In contrast, O–H stretching vibration peak intensity centered at 3480 cm^{-1} decreased from the OH group removal through cross-linking. The contact angle of deionized water on the film surface was measured as summarized in Table 1 [37].

AFM images of the insulator surface were obtained as shown in Fig. 3a–d. The film became rougher when more PMMF content was added with root-mean-square (RMS) roughness from 0.35 to 1.27 nm, which affected pentacene morphology. AFM images of 60 nm thick pentacene films on different dielectrics are displayed in Fig. 3e–h. The pentacene grain size showed decreasing trend from CEPM10 to CEPM70 because the surface roughness becomes a more