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Optimization of graphene-MoS_2 barristor by 3-aminopropyltriethoxysilane (APTES)

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ABSTRACT

We theoretically and experimentally investigated the influence of the Fermi level position of graphene relative to the Dirac point on the performance of a graphene/MoS_2 heterojunction barristor. A large Fermi level modulation ($\Delta E_F = 0.28$ eV) of graphene, when the V_{GS} is changed between −20 V and +20 V, was theoretically predicted when the Fermi level is located at the Dirac point. For reference, $\Delta E_F = 0.11$ eV when the Fermi level is far from the Dirac point. This prediction was experimentally proven using two kinds of barristors with pristine (strongly p-type) and 2.4% APTES-treated (intrinsic) graphene. The on/off-current ratio was improved by a factor of 32 (a 2.1-fold increase in the on-current density and a 15-fold increase in the off-current density) in the APTES-treated device, as compared to the control. Using a temperature-dependent current-voltage measurement, we quantitatively confirmed the larger modulation of the barrier height in the APTES-treated barristor ($\Delta E_F = 0.27$ eV) compared to that of the control device ($\Delta E_F = 0.14$ eV). This study can be used to guide the design and optimization of graphene-based heterojunction devices.

1. Introduction

Graphene has attracted significant interest for electronic applications because of its high carrier mobility [1], high thermal conductivity [2], superior mechanical flexibility [3], and optical transparency [4]. Recently, in order to resolve the low on/off-current ratio that is a critical weak point of graphene devices, graphene-based heterojunction barristors were proposed. These barristors are based on heterojunctions with other materials including hexagonal boron nitride (*h*-BN), molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), tungsten disulfide (WS_2), tungsten diselenide (WSe_2), indium gallium zinc oxide (IGZO), and pentacene [5–8,19,20]. The performance of these heterojunction graphene barristor devices must be investigated in more detail because the graphene layer on SiO_2 that is normally used as a gate dielectric in the above works suffers from a charge puddle effect [9–11], which eventually causes a strong *p*-doping phenomenon in the graphene. Charged impurities on SiO_2 and adsorbed polar molecules are known to cause strong p-type electrical properties in graphene [9]. Specifically, the charge puddle phenomenon seems to degrade the performance of graphene barristors by (*i*) reducing the carrier mobility in graphene and (*ii*) limiting the modulation of the Fermi level of graphene. Graphene's Fermi level modulation is predicted to be reduced because the Fermi level is located far from the Dirac point (due to the strong *p*-doping effect) where the density of states is very low. To overcome this limitation, researchers have suggested using suspended graphene; this material shows a significant improvement in the mobility but it is very delicate and makes device fabrication difficult [12]. As an alternative, self-assembled monolayer (SAM)-covered substrates have recently been explored in an attempt to block the charge puddle effect [9].

In this study, we theoretically and experimentally investigate the influence of the Fermi level of graphene relative to the Dirac point on the performance of graphene/MoS_2 heterojunction barristors. To block the charge puddle effect and recover the intrinsic properties of graphene, a 3-aminopropyltriethoxysilane (APTES) treatment is applied on the SiO_2 surface (where a large number of charged impurities and adsorbates exist). Finally, through temperature-dependent current-voltage measurements, we quantitatively study the change in the barrier height as a function of the applied gate voltage in graphene/MoS_2 barristor devices fabricated with pristine or APTES-treated graphene. The pristine graphene is

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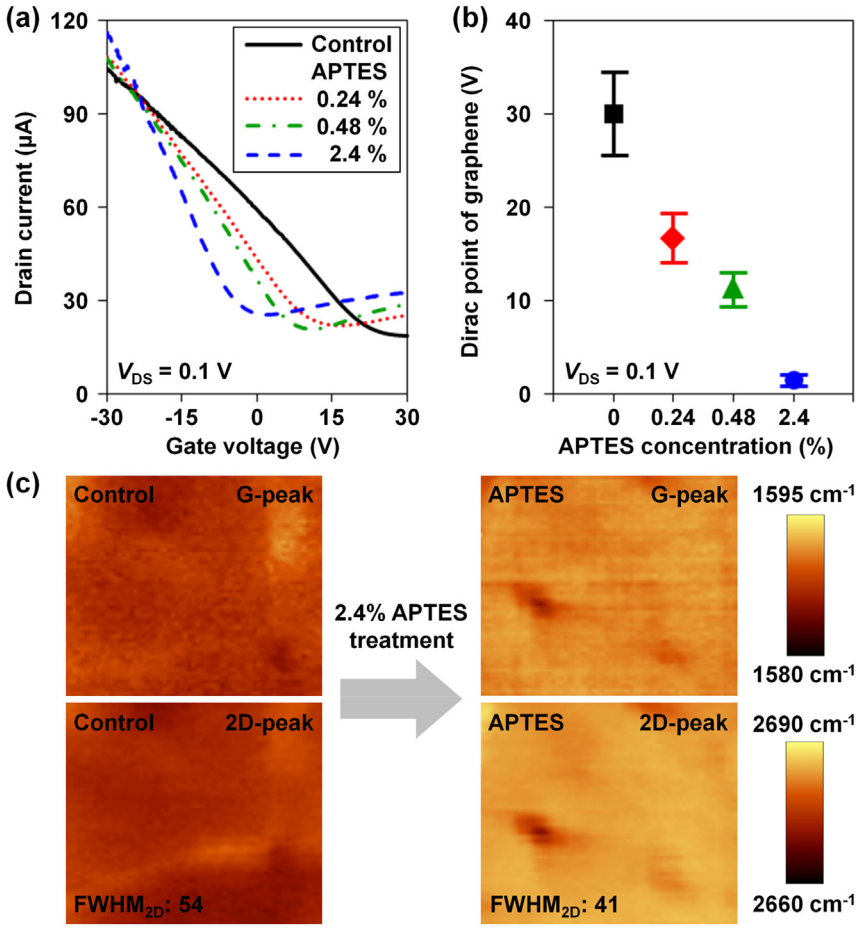

Fig. 1. (a) I_D-V_G characteristics of pristine, 0.24%, 0.48%, and 2.4% APTES-treated graphene transistors at $V_{DS} = -0.1$ V. (b) Dirac points as a function of the APTES concentration, which were extracted from the pristine, 0.24%, 0.48%, and 2.4% APTES-treated graphene device samples. Raman mapping images of the G and 2D peaks in (c) pristine and 2.4% APTES-treated graphene layers.

strongly influenced by charged impurities (p-type), while the APTES-treated graphene is unaffected by the charge puddle effect (intrinsic).

2. Experiments

To perform APTES treatment on SiO_2/Si substrates, different amounts of APTES (60 μL, 120 μL, and 600 μL) were added to 25 mL of toluene. SiO_2/Si substrates were soaked in these solutions for 1 h. Next, the samples were rinsed and sonicated for 10 min using toluene, alcohol, and deionized water. This was followed by a baking process at 120 °C for 20 min. To fabricate graphene back gated transistors, graphene was grown on copper (Cu) foil by a chemical vapor deposition method. Poly(methyl methacrylate) (PMMA) was spin-coated on the graphene/Cu foil, and the Cu foil was etched in ferric chloride ($FeCl_3$). Using a wet transfer method, the graphene was then transferred onto highly-doped Si substrates with a 90-nm-thick layer of bare SiO_2 or onto APTES-treated SiO_2. The PMMA was then removed in acetone for 3 h. The transferred graphene was patterned by photolithography and oxygen plasma etching processes to define the active channel region with a width of 100 μm and a length of 25 μm. Finally, the source/drain regions were defined by photolithography, and Ti/Au (10/30 nm) layers were deposited with an electron-beam evaporation system. Both pristine and APTES-treated graphene samples were analyzed through electrical measurements via a Hewlett-Packard (HP) 4155A semiconductor parameter analyzer at room temperature and Raman spectroscopy using a WITec micro-Raman spectrometer system. To fabricate graphene/MoS_2 heterojunction barristors, MoS_2 flakes were mechanically exfoliated onto PMMA/polyvinyl alcohol (PVA)-coated Si substrates with blue Nitto tape. After exfoliation, the samples with MoS_2 flakes were dipped in deionized water to dissolve the PVA layer. This resulted in a MoS_2/PMMA layer floated on deionized water, which was subsequently transferred onto a patterned graphene sample through a dry transfer technique [13]. The PMMA layer was then removed by soaking in acetone for 3 h. The source and drain electrodes, which consisted of Ti (10 nm) and Au (30 nm), were formed by lithography, evaporation, and lift-off processes. We then conducted electrical measurements on both the pristine and APTES-treated graphene/MoS_2 heterojunction barristors using an HP 4155A semiconductor parameter analyzer. The temperature-dependent electrical characteristics were also measured between 340 K and 160 K.

3. Result and discussion

Fig. 1(a) shows the electrical characteristics of graphene transistors fabricated on the pristine (control) and APTES-treated graphene layers. The extracted Dirac points are plotted as a function of the APTES concentration in Fig. 1(b). The Dirac point of the control graphene device was observed at ~30 V (because of the charged impurities on the SiO_2 surface and the adsorbed polar molecules),