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Effects of film microstructure on the bias stability of pentacene field-effect transistors

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ABSTRACT

In this report, the effects of film microstructure on the bias stability of pentacene field-effect transistors (FETs) were investigated. To control the microstructure of pentacene film, substrate temperature was changed from 25 to 90 °C during pentacene deposition. As the substrate temperature increased, pentacene grain size increased (or grain boundary (GB) decreased) because of the elevated surface diffusion of pentacene molecules. Accordingly, field-effect mobility increased up to 1.52 cm^2/V. In contrast, bias stability showed totally different characteristics: samples prepared at high substrate temperatures exhibited the lowest degree of bias stability. This GB independent charge trapping phenomenon was solved by examining molecular scale ordering within the intragrain regions. The pentacene film grown at 90 °C showed the largest percentage of pentacene molecules with bulk crystalline structures. This inhomogeneity in the pentacene microstructure induces crystal mismatch within intragrain region, thereby providing deep trap sites for gate-bias stress driven instability. Our study shows that GB is not the main sites for bias stress related charge trapping, rather the molecular orientation within intragrain region is responsible for the charge trapping events. In this regard, the control of molecular scale ordering is important to obtain OFETs with a high bias stability.

1. Introduction

Organic field-effect transistors (OFETs) have received considerable attention as a switching element in the future display backplane [1–3]. Because continuous bias is applied to OFET devices, bias stability is one of the required performance parameters before their commercialization [4–6]. In p-type OFETs, ON-bias (namely, negative gate bias) typically leads to a shift of their transfer curve to a negative gate voltage direction. This behavior is consistent with the bias-stress effect observed in a-Si:H FETs and generally explained by charge trapping. Gate-bias is screened by trapped charges, thereby resulting in a negative shift in the threshold voltage (or decrease in the ON current). Although several models such as the formation of bipolaron and migration of mobile ion were proposed, the origin of the bias instability has not yet been fully understood [7–10]. Moreover, there exists a dispute on the charge trapping sites where charge trapping occurs. In common, semiconductor, dielectric, semiconductor–dielectric interface, and source/drain contact region are responsible for charge trapping sites [6].

Among these four regions, charge trappings at the semiconductor were previously demonstrated by several research groups, and light induced releasing of bias stress was regarded as an indicator of the bias stress driven charge trapping at the semiconductor [11]. Single crystalline organic semiconductor free of defects and disordered regions is reported to show strong resistance to bias stress [12]. However, single crystals can be grown under well-controlled conditions, and the applications of single crystals in real FET device needs additional transfer (or positioning) steps [13]. Instead, most organic semiconductors exhibit polycrystalline nature. In this polycrystalline film, mesoscale order such as grain boundary and crystalline domain can exist. Furthermore, molecular scale order can be significantly changed by adopting different crystal structures. In thermally evaporated pentacene film, for example, the polymorphism (i. e., thin-film phase, bulk phase) adds more complexity in the structural characterization [14,15]. Previous reports mainly focused on finding the relationship between these meso/molecular scale order and field-effect mobility

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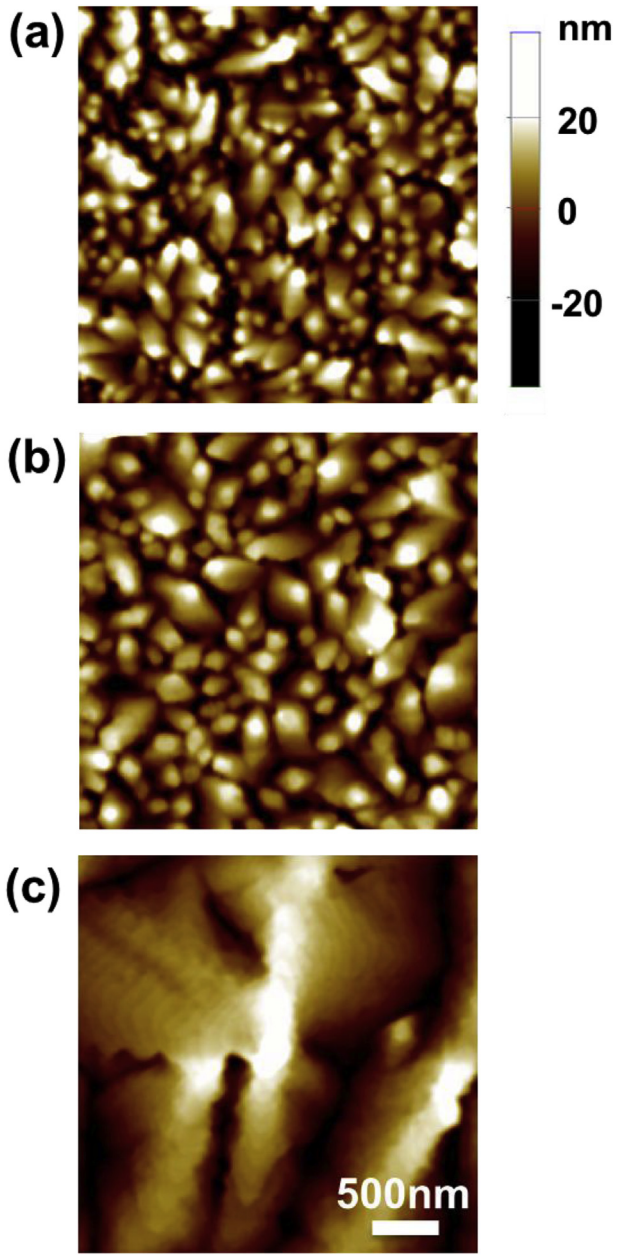

Fig. 1. AFM images of the pentacene films deposited at various substrate temperatures: (a) 25 °C, (b) 60 °C, and (c) 90 °C.

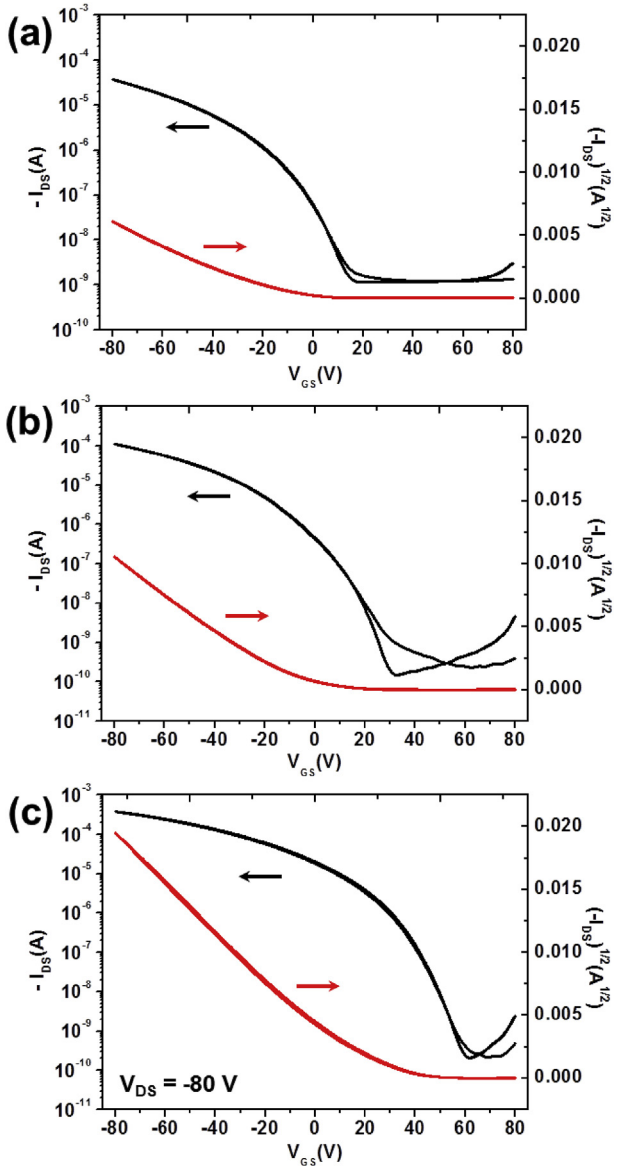

Fig. 2. Transfer characteristics of the FETs based on pentacene films deposited at various substrate temperatures: (a) 25 °C, (b) 60 °C, and (c) 90 °C.

[16,17]. However, only a small number of studies has been conducted to examine the inter-relationship between these meso/molecular scale order and bias stability. Although several studies indicated that the increase in crystallinity increases the bias stability, the effects of grain boundary (GB) and molecular orientation on the bias stability have not yet been examined [18,19]. Thus, microstructure dependent charge trapping exclusively related to bias stability need to be clarified among various types of charge trapping behaviors within organic semiconductors.

In this study, the bias stability of FETs based on pentacene films with different microstructures was investigated. To control the grain size and molecular orientation within pentacene grains, substrate temperature was changed from room temperature (25 °C) to 90 °C during pentacene evaporation. Common device characteristics (i. e., field-effect mobility) were extracted from the transfer curves, whereas gate bias stabilities were analyzed from the shifts in the transfer curves under continuous gate bias. Finally, the obtained bias stabilities were correlated to the microstructures of pentacene films.

2. Experimental section

Pentacene was purchased from Sigma–Aldrich (triple-sublimed grade, ≥99.995%). SiO_2 (thickness of 300 nm)/Si substrates were cleaned with acetone prior to use. Pentacene films of thickness ~50 nm were thermally evaporated on SiO_2/Si substrates. During the evaporation of pentacene, substrate temperature was fixed at room temperature (25 °C), 60 °C, and 90 °C. Atomic Force Microscopy (Park Scientific Instrument, Autoprobe-PC) was used to characterize the morphologies of the 50-nm thick pentacene films. Two-dimensional grazing-incidence X-ray diffraction (2D-GIXRD) patterns were recorded in Pohang Accelerator Laboratory of Korea (9A [wavelength: 1.121 Å] and 3C [wavelength: 1.2096 Å]