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Organic Electronics 8 (2007) 455–459
Organic Electronics
www.elsevier.com/locate/orgel

Letter

Improved pentacene device characteristics with sol–gel SiO_2 dielectric films

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Received 13 November 2006; received in revised form 20 December 2006; accepted 20 December 2006
Available online 29 December 2006

Abstract

The interfacial interactions between semiconductors and gate dielectrics have a profound influence on the device characteristics of field effect transistors (FETs). This paper reports on the concept of introducing a sol–gel SiO_2 as inorganic capping layer to significantly improve device characteristics of pentacene-based FETs. The smoother film surfaces of sol–gel SiO_2 (1.9 Å root-mean-square) induced larger pentacene grain sizes, and led to hole mobilities of 1.43 cm^2/Vs, on–off ratio of 10^7, and a subthreshold swing of 102 mV/decade when operating at −20 V.
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PACS: 72.80.Le; 81.20.Fw; 82.35.Gh; 85.30.Tv

Keywords: Pentacene; Field effect transistors; Sol–gel; Dielectrics

1. Introduction

Research into organic field effect transistors (OFETs) has gained great interest because of their potential applications in low-cost and large area electronics [1–7]. For pentacene-based FETs, better device performances have been achieved by tuning the film deposition rate, substrate temperature, material purity, and substrate surface. However, the electronic transport, in particular the role of semiconductor–dielectric interfacial interactions, of the polycrystalline films is still poorly understood [3–5]. Thermally grown SiO_2 as the gate dielectric is a widely used substrate for the growth of pentacene, mainly due to its superior electrical properties. However, for large area electronics applications, organic electronics on glass or flexible foil substrates, solution processed organic or inorganic dielectrics are imminent [6].

Candidates for large area compatible inorganic dielectrics are sputtered silicon oxide, sputtered Al_2O_3, or plasma-enhanced chemical vapor deposited

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doi:10.1016/j.orgel.2006.12.006

(PECVD) silicon nitride and silicon oxide. These dielectrics require complex and expensive processes, higher temperatures, and are not compatible with low-cost, solution processed methodologies. Solution processed organopolysilsesquioxane glass resins (GR) as gate dielectrics, with moderate improvement in device characteristics, have been reported [7]. Sol–gel based process high-*k* dielectrics have also been proposed [8,9], however concerns over roughness [10] and interfacial compatibility with pentacene remain [11]. The present paper reports on the possibility of using sol–gel SiO_2 film as a capping/surface modification layer that can significantly improve FET device characteristics. Electrical properties between pentacene on thermally grown SiO_2 and sol–gel SiO_2 bi-layer films are compared. Bi-layer approaches have been shown to allow effective modification of bottom layer topography without being limited by the chemistry required for self-assembled monolayer (SAM) functionalization, while simultaneously fine-tuning the dielectric surface [12]. The surface of the sol–gel SiO_2 film was found to be smoother than thermally grown SiO_2, resulting in planarization of dielectric surface roughness. This results in higher mobility of up to 1.43 cm^2/Vs for pentacene on sol–gel SiO_2 due to larger grain size.

2. Experimental details

Sol–gel SiO_2 films with excellent uniformity were prepared by a two-step acid–base catalyst procedure and spin coating. This process allows the completion of polycondensation at low temperatures and the development of silica networks during drying and post-treatment [13]. Sol–gel solutions were prepared by mixing tetraethylorthosilicate (TEOS, 99.9% purity), ethanol, ammonium hydroxide, deionized water and concentrated HCl. In the first step, TEOS, ethanol, water, and HCl were stirred at room temperature for 90 min in the following molar ratios: 1:10:3.5:0.003. Three drops of the base catalyst (0.1 M NH_4OH) was then added to the above solution. Solution was aged under constant stirring at room temperature for 3 days.

The pentacene FETs were fabricated on n-type Si/thermally grown SiO_2 (450 Å). All substrates were cleaned by wet cleaning procedures (Piranha solution, SC2, and SC1). Sol–gel SiO_2 solution was spin-coated (2000 rpm) on the substrate to form the bi-layer dielectric sample (Fig. 1, Device II). Sol–gel films were dried at ambient conditions at 60 °C

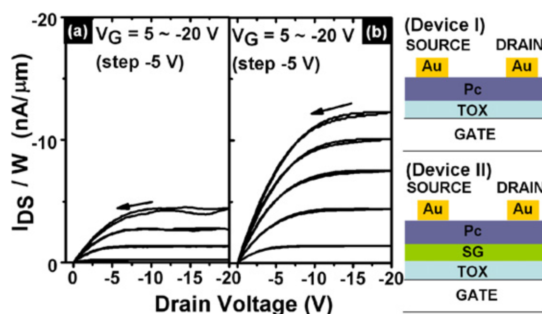

Fig. 1. Drain current–drain voltage (I_{DS}–V_{DS}) curves obtained from pentacene-based FETs with (a) thermally grown SiO_2 uni-layer film (Device I), (b) sol–gel SiO_2-thermally grown SiO_2 bi-layer film (Device II). [Gate = n-type Si wafer, TOX = thermally grown SiO_2, SG = sol–gel SiO_2, Pc = pentacene].

and were further heated at 100 °C, 10^{-7} mbar, before pentacene deposition. The 500 Å pentacene (sublimed once) film was evaporated under a vacuum of 10^{-7} mbar. During the deposition, the substrate temperature was held at 100 °C and the deposition rate was sustained at 0.5 Å/s. Gold source and drain layers were patterned using a shadow mask. The thickness of the sol–gel SiO_2 film was 3900 Å. The capacitance of 76.7 and 17.1 nF/cm^2 was measured on uni-layer (Fig. 1, Device I) and bi-layer structures respectively, through the capacitance–voltage method using HP4284 LCR meter. The transistor characteristics were measured using Keithley 4200 semiconductor parameter analyzer. All electrical measurements were done in Desert Cryogenics probe station with a base pressure of 5×10^{-5} mbar.

3. Results and discussion

Contrary to that of the reference FETs, saturation of the drain current was not observed in bi-layer FETs (Fig. 1b). This can be attributed to the reduced electric field across the gate dielectric in the bi-layer FETs as compared to the uni-layer devices (Fig. 1a). At $V_G = -20$ V, the gate electric fields were 0.98 MV/cm and 4.44 MV/cm in the bi-layer TFT and uni-layer FETs respectively, calculated using the equivalent oxide thickness (EOT). Therefore, the channel saturation that typically ensues at high electric fields had not occurred in the bi-layer FETs. Despite its lower gate dielectric field, bi-layer FETs display higher I_{DS} than that of uni-layer FETs.

Saturation mobility, μ_{sat}, may be extracted from the saturation region of the transfer characteristics (Fig. 2) as follows:

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