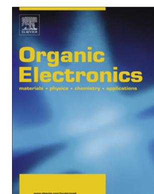
Organic Electronics 15 (2014) 937–942

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel



Accounting for variability in the design of circuits with organic thin-film transistors

Kris Myny [a,*], Pieter van Lieshout [b,1], Jan Genoe [a,c], Wim Dehaene [a,c], Paul Heremans [a,c]

[a] Imec, 3001 Leuven, Belgium
[b] Polymer Vision, Eindhoven, The Netherlands
[c] KULeuven, ESAT Department, Kasteelplein 10, 3001 Leuven, Belgium

ARTICLE INFO

Article history:
Received 23 September 2013
Received in revised form 24 January 2014
Accepted 26 January 2014
Available online 7 February 2014

Keywords:
Variability
Organic electronics
Organic circuits
RFID
Pelgrom
Mismatch
TFT
Thin-film transistor
Yield

ABSTRACT

We experimentally verify that the methodology to account for local parameter variations and transistor mismatch known in Si CMOS technologies can be transposed to organic thin-film transistor technologies, and we present a design case that makes use of design for variability. Transistor parameter variation decreases with the square root of the transistor footprint. As a consequence, Monte Carlo simulations which take this effect into account can be executed to better predict the final circuit yield. The design case in this work is an 8-bit, organic RFID transponder chip. The yield prediction by simulations corresponds to the finally observed circuit yield.

© 2014 Elsevier B.V. All rights reserved.

1. Introduction

Process variations present during transistor fabrication lead to a certain variability on the resulting transistor parameters. Current and upcoming process nodes for Si-CMOS technologies are such an example where parameter variability increases substantially with subsequent nodes due to downscaling of the device dimensions towards the limits of the technology [1–5]. Also ultra-low power circuit designs based on subthreshold logic are very sensitive to transistor variations [6–9]. Considerable parameter variations have been reported for organic thin-film transistors [10–13]. These variations find their origin in the organic materials employed and the rather immature, often printing, technology. They have an impact on one or more parameters of the saturation current equation of thin-film transistors (Eq. (1)).

$$I_{DS,sat} = \frac{1}{2}\mu\frac{\varepsilon_r\varepsilon_0}{t_i}\frac{W}{L}(V_{GS}-V_T)^2 \qquad (1)$$

where V_T, W, L, μ, ε_r and t_i have their usual meaning [14]. Variations in the threshold voltage V_T affect the saturation current of the transistor quadratically, while variations in μ, $C_i = \frac{\varepsilon_r\varepsilon_0}{t_i}$ and device geometry influence the saturation current only linearly. This work focuses on within-die or intra-die (WID) variations, which are categorized as deviations of the transistor parameters in the same die, equal to the size of the designed chip. At first, we will demonstrate dependencies of parameter variation with respect to the geometric size of the transistor. We report a similar behavior as observed for Si-CMOS technologies. These results will be used to obtain an improved yield prediction by

* Corresponding author.
E-mail address: kris.myny@imec.be (K. Myny).
[1] Current address: ASML, Veldhoven, The Netherlands.

http://dx.doi.org/10.1016/j.orgel.2014.01.020
1566-1199/© 2014 Elsevier B.V. All rights reserved.

means of the design case based on an 8-bit organic RFID transponder chip.

2. Mismatch modeling

Local or within-die variations can be analyzed by running Monte Carlo (MC) circuit simulations. MC simulations perform a number of subsequent circuit simulations, whereby, for each simulation run, the selected parameters (like V_T) are distributed randomly across all transistors according to predefined mean and spread values. By performing a multitude of MC runs, the yield of the evaluated circuit can be estimated. This analysis tool is available in SPICE. As a starting point, it is very important to have detailed data on WID variations of the targeted technology. The technology of this work has been developed by Polymer Vision for commercialization in rollable active matrix displays [15]. Fig. 1 depicts the transfer characteristics operated in saturation regime, representing the nominal value of V_T for this technology. The solid line shows the measured curve after TFT fabrication and the dashed line represents the corresponding fit (e.g. from a low-level spice model) as generated by the circuit simulator.

Since this technology has been developed for display applications, the absolute value and the spread on on-state current at large negative V_{GS} are key parameters. Fig. 2 depicts the ratio between standard deviation on I_{on} and average I_{on} versus the transistor area, obtained for this technology. This data is collected for five 150 mm wafers. Around 130 different transistors have been measured for five different transistor sizes, namely 7/5, 14/5, 28/5, 56/5 and 140/5. The TFT layout is included in Fig. 2. For all sizes, the only change in layout is the size of the semiconductor island. The other layers in the device layout remain unaltered. We observe that the percentage of spread in I_{on} increases linearly with decreasing square root of transistor area, apart from the smallest transistor size (7/5). We assume that edge effects are dominant for the smallest TFT with a semiconductor island width of only 3.5 μm, compared to larger devices.

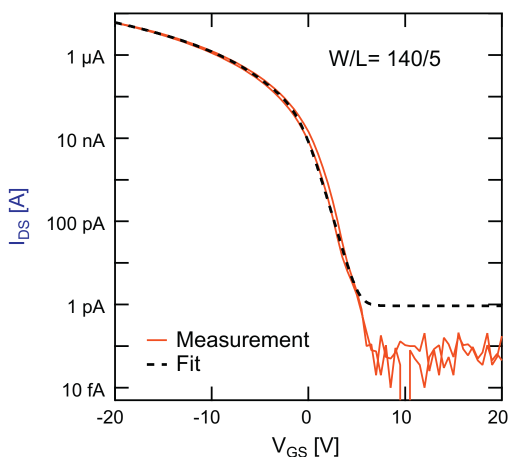


Fig. 1. Transfer characteristics of an organic transistor on foil operated in saturation regime, with W/L of 140/5. The full line shows the obtained mean curve, while the dashed line represents the corresponding fit.

A possible explanation for this effect suggests averaging of process variations with increasing area. For Si-CMOS technologies, Pelgrom et al. have derived in 1989 a model for matching properties of MOS transistors [16]. They concluded that the variance of the threshold voltage and the current factor β, being $\mu C_i W/L$ between two adjacent and closely spaced devices are inversely proportional to the transistor area.

The data in this work evaluates the variance for single devices, contrary to Pelgrom's model which calculates the mismatch between two devices. The difference between both approaches is explained in Eq. (2) using the threshold voltage as an example. The variance of the difference in threshold voltage for two devices (distributed randomly) is the sum of their individual variances. There is a factor 2 difference between both approaches. In this work, for WID variations, we use the standard deviation of the absolute parameter.

$$\sigma^2(\Delta V_T) = \sigma^2(V_{T,TFT1}) + \sigma^2(V_{T,TFT1}) = 2\sigma^2(V_T) \quad (2)$$

The dashed line in Fig. 2 corresponds to a linear fit based on the measured data, leading to general Eq. (3).

$$\frac{\sigma^2(I_{on})}{\overline{I_{on}}^2} = \frac{A^2_{I_{on}}}{WL} + K1 \quad (3)$$

$A_{I_{on}}$ is an area proportionality constant for I_{on} and $K1$ is a constant factor. As a consequence, the first part of this equation suggests that Pelgrom's mismatch law may also be valid for organic TFTs. The second part of the equation and Fig. 2 shows also a non-zero variability for infinite area, represented in Eq. (3) by $K1$. This suggests that the data collected on the full 150 mm wafers suffers also from die-to-die variation. Eq. (8) of Pelgrom's paper includes a distance-dependent parameter taken into account the effect of long-correlation distance variations [16]. In the next part of this work, we will shift from full 150 mm wafer analysis to closely-spaced devices focusing on WID variations, where the distance parameter of Pelgrom's equation (8) may be excluded. As a consequence, Eq. (3) will be simplified by eliminating term $K1$.

140/5 is selected as the smallest TFT for circuit realization in this technology, integrated as the drive TFT in a zero-V_{GS}-load logic gate. Fig. 3(a) shows an example of WID variations, obtained from 16 measured transistors with W/L of 140/5. These transistors are distributed with a pitch of 500 μm horizontally and 650 μm vertically. The extracted standard deviation for the threshold voltage is 0.35 V for a 140/5 transistor, which is a typical value extracted for this technology. The inset of Fig. 3(a) depicts the corresponding V_T distribution for all measured transistors. This indicates a Gaussian distribution of V_T is present and that MC simulations can be performed using this Gaussian distribution. Fig. 3(b) is the results of 40 MC simulation runs in the circuit simulator, including standard deviations on charge carrier mobility and threshold voltage. A good correspondence is observed.

Similar analysis has been made for a transistor with an increased geometry, namely 1400/5. This is the chosen load transistor for our zero-V_{GS}-load inverters and NAND-gates. Fig. 4 plots the measured and simulated WID variations of

Download English Version:

https://daneshyari.com/en/article/1264439

Download Persian Version:

https://daneshyari.com/article/1264439

Daneshyari.com