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# Tunable contact resistance in double-gate organic field-effect transistors

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ABSTRACT

A study of the contact resistance ($R_{sd}$) in pentacene-based double-gate transistors is presented. In top-contact transistors, as the negative bias of the additional top-gate bias is increased, $R_{sd}$ decreases by over five orders of magnitude for small bottom-gate voltages. In bottom-contact transistors, $R_{sd}$ is reduced by about ten times for all bias values, implying improved charge transport in all operating regimes. The different tunability of $R_{sd}$ in top/bottom-contact transistors is attributed to different charge injection modulation by the coplanar/staggered top gate. Therefore, double-gate architecture offers a novel and effective approach to limit $R_{sd}$ and its relevant impacts on organic transistor.



## 1. Introduction

Organic field-effect transistors (OFETs) are fast evolving towards a variety of potential applications; however, they still suffer from low carrier mobility and low stability. In attempts to improve the performance of OFETs, most past efforts have concentrated on the organic semiconducting materials and less attention has been paid to the devices themselves. Recently, double-gate or dual-gate (DG) OFETs have attracted considerable interest in the research community [1–12]. In addition to the single gate electrode present in conventional OFETs, a second gate electrode is added in DG OFETs. This does not significantly increase technological complexity and device size but enables higher mobility [1,5], adjustable threshold voltage [2,3,7,8], higher $I_{on}/I_{off}$ ratio and better sub-threshold characteristics [3,4,9]. Logic circuits, displays, memory and sensors based on DG OFETs have also been demonstrated [11,13–15]. In contrast to the intensively studied mobility and threshold voltage, a comprehensive study of the contact resistance ($R_{sd}$) in DG OFETs is still lacking. In fact, the contact resistance is closely related to the OFET operating mechanisms and its analysis can help us to explore how the DG OFETs work. Moreover, the contact resistance has always been a crucial issue in OFETs due to the strong limitation to transistor performance, particularly with significant device miniaturization [16]. In this regard, the double-gate architecture is expected to be a novel and effective means of reducing the contact resistance. With these considerations in mind, in the present study we systematically investigate the contact resistance in pentacene-based DG OFETs.

## 2. Experimental

The top-contact (TC) and bottom-contact (BC) OFETs used in this work are schematically illustrated in Fig. 1a and b, respectively. They were fabricated on heavily doped Si (100) wafers covered with a 50-nm-thick $SiO_2$ layer, which serve as the common bottom gate (BG) electrode and the BG insulator, respectively. After the surface was

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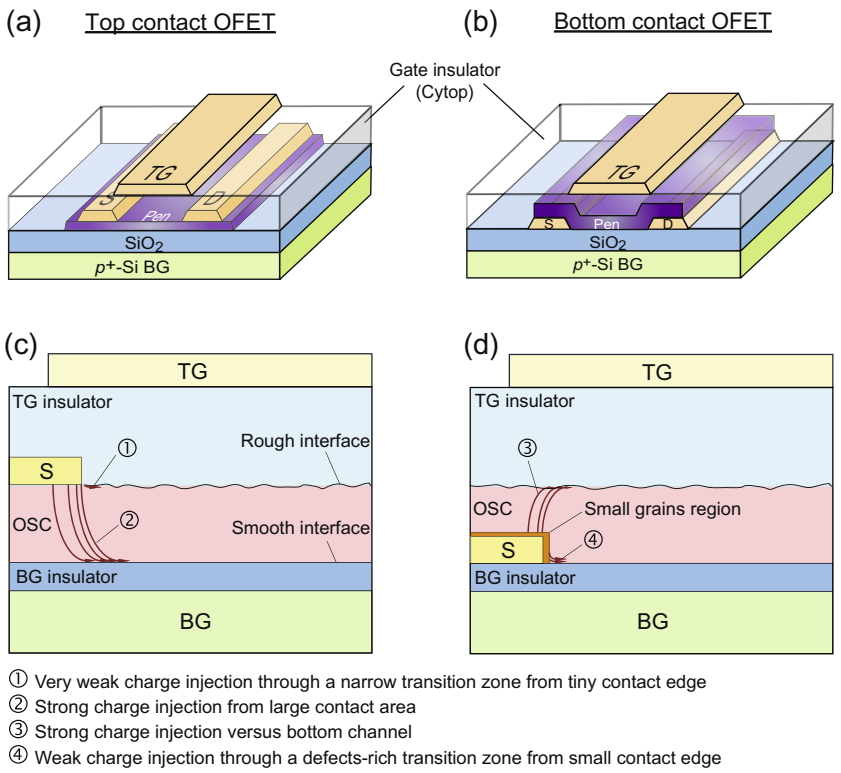


**Fig. 1.** (a and b) Schematic illustration of TC and BC double-gate OFETs, respectively. (c and d) Close-up of the source contact in TC and BC double-gate OFETs, respectively, where the TG/BC gate electrodes are negatively biased.

ultrasonically cleaned with acetone and isopropyl alcohol, the substrates were immersed in a mixture of sulfuric acid and hydrogen peroxide to fully remove organic contaminants. Following that, the substrates were immersed in a 10 Mmol chloroform solution of phenethyltrichlorosilane (PhTS) to form a self-assembled monolayer (SAM) on the $SiO_2$ surface. For BC OFETs, the source and drain electrodes were deposited directly on the PhTS pre-treated $SiO_2$ surface. This was achieved by sequential evaporation of 3-nm-thick Ti and 40-nm-thick Au layers through a metal mask with channel length $L = 50\ \mu m$–$350\ \mu m$ (interval of 50 μm) and uniform channel width $W = 1000\ \mu m$, where Ti used as an adhesion layer. Next, a pentacene (Aldrich, purified using temperature gradient sublimation) layer was vacuum-deposited (rate of 0.01 nm/s at room temperature, thickness of 40 nm). In the TC devices, the pentacene layer was deposited first and then the source and drain electrodes were formed by thermal evaporation of Au through a metal mask. To produce the top gate (TG) dielectric layer, pure Cytop™ (Asahi Glass) was spin coated on the previously obtained conventional TC/BC OFETs, first at 500 rpm for 5 s and then at 4000 rpm for 60 s, forming a 535-nm-thick TG insulator as confirmed by a surface profiler (KLA Tencor P-16+). Finally, the TG electrode was formed by thermal evaporation of a 40-nm-thick Au layer through a metal mask by optical alignment. Current–voltage ($I$–$V$) characterizations were carried out in vacuum at room temperature using a HP4156c semiconductor parameter analyzer. For small drain voltages, no nonlinear behavior in the output characteristics was observed, implying nearly ohmic contacts. The maximum leakage current for both gates was found to be about $10^{-8}$ A/cm$^2$, thus ensuring the reliability of the subsequent analyses.

## 3. Results and discussion

### 3.1. Top-contact OFETs

We first examined the TC OFETs with the TG electrode left floating. The intrinsic low-field mobility $\mu_0$ and the threshold voltage $V_T$ for the bottom channel were found to be $\mu_{0,bottom} = 0.2 \pm 0.03$ cm$^2$/Vs and $V_{T,bottom} = -1.5 \pm 0.5$ V where the unit-area capacitance of the BG dielectric $C_{i,bottom} = 8.0 \times 10^{-8}$ F/cm$^2$ for 50-nm-thick $SiO_2$. Here $\mu_0$ is evaluated by the Y function method and free from the contact resistance influences [17]. This intrinsic mobility reflects well the charge transport properties in the channel, thus it can be safely used for the next discussion.

We next analyzed the top channel with the BG electrode left floating, and obtained $\mu_{0,top} = 0.001$–$0.002$ cm$^2$/Vs ($C_{i,top} = 3.3 \times 10^{-9}$ F/cm$^2$ for 535-nm-thick Cytop) and $V_{T,top} = -2.0 \pm 1.0$ V. It can be seen that $\mu_{0,top} << \mu_{0,bottom}$ (TC) [2,9] and we will next see a completely different situation in BC OFETs where $\mu_{0,top} > \mu_{0,bottom}$ (BC) [1,10]. Note that the TG was fabricated using the same process for the TC and BC OFETs. After a thorough examination we found that a lower mobility was always observed in the coplanar