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Characterization of ohmic contacts in polymer organic field-effect transistors

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ABSTRACT

It is well known that contact resistance R_c limits the performance of organic field-effect transistors (OFETs) that have high field-effect mobilities ($\mu_{FET} \gtrsim 0.3$ cm^2 V^{-1} s^{-1}) and short channel lengths ($L_{ch} \lesssim 30$ μm). The usual transfer-line method (TLM) to analyze R_c calls for extrapolation of total resistance to zero L_{ch} at constant drain and gate voltages. This requires an unrealistic assumption that R_c does not vary with source–drain current I_{sd} (nor with channel carrier density σ). Here we describe a self-consistent TLM analysis that instead imposes the condition of constant I_{sd} and σ. The results explicitly reveal the dependence of R_c on I_{sd} and σ. We further describe how this $R_c(I_{sd}, \sigma)$ surface can be modelled to yield the specific contact resistivity ρ_c of the metal/organic semiconductor (OSC) interface, a key parameter that has so far been neglected in OFETs. We illustrate the application of these analyses to high-performance staggered top-gate bottom-contact poly(2,5-bis(alkyl)-1,4-dioxopyrrolo [3,4-c]pyrrole-3,6-diyl-terthiophene-2,5″-diyl) (DPPT2-T) OFETs fabricated on bottom Au source–drain electrode arrays, with high contact-corrected μ_{FET} of 0.5 cm^2 V^{-1} s^{-1}. We show that when these electrodes are modified to impose weak, and then strong hole-doping of the DPPT2-T interface, R_c diminishes and its dispersion, i.e. dependence on I_{sd} and σ, weakens. The ultimate ρ_c attained for the strongly hole-doped contact is *ca.* 1 Ω cm^2, broadly independent of I_{sd} and σ, which we propose is a hallmark of a true metal/OSC ohmic contact. For comparison, the bare Au/DPPT2-T contact gives ρ_c of the order of 10 Ω cm^2 with a marked σ dependence. The lowest ρ_c reached here shortens the current transfer length down to *ca.* 5 μm, enabling short electrode lengths to be advantageously employed in technology.

1. Introduction

The performance of OFETs has vastly improved over the past decade or so primarily due to the emergence of OSCs with high $\mu_{FET} \gtrsim 0.3$ cm^2 V^{-1} s^{-1} [1,2]. Consequently R_c has been recognized since a decade ago as a key performance bottleneck for transistor dimensions and geometries of technological relevance. The presence of a large R_c decreases the apparent transistor mobility and speed, increasing the stage delay of digital circuits [3]. Yet the nature of R_c in OSC devices and how to reduce this in practical technologies have not been well understood despite immense interest. The total resistance (width-normalized; typical units, Ω cm) across the transistor operated at drain–source voltage V_{ds}, gate–source voltage V_{gs} and source–drain current I_{sd} is given by:

$$R_{tot} = R_{ch} + R_c, \tag{1}$$

where R_{tot} is given by $V_{ds}/-I_{sd}$, R_{ch} is the channel resistance, and $R_c = \sum_{i=s,d} R_{c,i}$ is the contact resistance summed over both source

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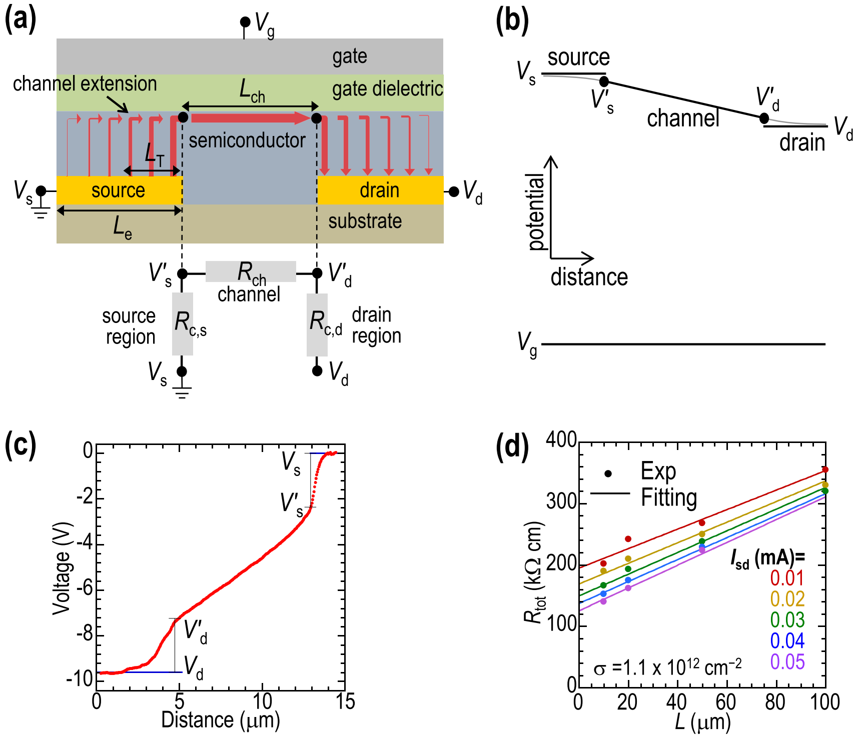

Fig. 1. Evaluation of R_c as a function of (I_{sd}, σ) using the transmission-line model. (a) Schematic of the TLM and terminology employed in this report. **(b)** Schematic of the electrostatic potential profile along the semiconductor/dielectric interface of the OFET. **(c)** Measured potential profile across the channel of a BGBC C_{14}-PBTTT OFET with Au contacts using atomic-force-microscope potentiometry. Resolution, 100 nm; channel length, 9 μm. Vertical bars indicate the contact voltage drops. **(d)** Example R_{tot} *vs* L_{ch} plots to find R_c from the $L_{ch} = 0$ intercepts for different I_{sd} at mean $\sigma = 1.1 \times 10^{12}$ cm^{-2} for PEDT:PSSH-coated Au as source–drain contacts, with DPPT2-T as semiconductor, and 490-nm thick polystyrene as gate dielectric. The global fits are for constant $\mu_{FET} = 0.45$ cm^2 V^{-1} s^{-1}. The slopes vary slightly because of the small variation in σ about the mean value.

(i = s) and drain (i = d) electrodes (Fig. 1a). This R_c is well defined and meaningful for contacts to doped semiconductors, and to undoped semiconductors supporting space-charge-limited-current (SCLC) conduction. I_{sd} passes along the transistor channel and through both contact regions. This cannot be directly measured, but inferred from source current I_s or drain current I_d after leakage correction. The contact region comprises the electrode/semiconductor contact and the intervening semiconductor layer bridging to the channel. The low R_{ch} that can now be achieved in the transistor "on" state requires R_c to be even lower so that the transistor performance is not limited by the contacts [4].

Since R_{ch} is proportional to L_{ch} and inversely proportional to μ_{FET}, the demand on R_c has become particularly severe at high μ_{FET} and short L_{ch}. For example, a *p*-type OFET with $L_{ch} \approx 30$ μm and $\mu_{FET} \approx 0.3$ cm^2 V^{-1} s^{-1}, operating at $\sigma \approx 1.0 \times 10^{12}$ hole cm^{-2}, has an "on" state $R_{ch} \approx 60$ kΩ cm. Therefore R_c needs to be much lower than this value in order to not limit performance. This turns out to be challenging even for the staggered device configurations, i.e. top-gate bottom-contact (TGBC) and bottom-gate top-contact (BGTC) OFETs, let alone the in-plane configurations, i.e. top-gate top-contact (TGTC) and bottom-gate bottom-contact (BGBC) OFETs which additionally suffer from current crowding at the contact edges [4].

In our search for new general methods to reduce R_c, we realized it is necessary to also develop a better analysis and understanding of R_c. Much of the work over the past decade has focused on characterizing the dependence of R_c on V_{ds} and V_{gs} to given in effect the $R_c(V_{ds}, V_{gs})$ surface. Several techniques have been developed and refined, including the TLM [5–8], gated four-probe (GFP) measurements [9–13] and scanning potentiometry [14–16], with TLM the technique of choice by far for *in device* characterization since it requires only a set of L_{ch} rather than special structures, and is not limited to a particular device configuration [17].

For reasons of simplicity however, R_c has been conventionally obtained by extrapolation of R_{tot} to zero L_{ch} at constant (V_{ds}, V_{gs}). This requires $\partial R_c / \partial L_{ch}|_{(V_{ds},V_{gs})} = 0$. For R_c to remain constant as L_{ch} increases, R_c needs to be independent of I_{sd}, since I_{sd} decreases as L_{ch} increases while (V_{ds}, V_{gs}) is held constant. This prerequisite cannot be met in general, and so this approach is fundamentally flawed. Readers may wish to look ahead to Fig. 3 to see examples of the explicit dependence of R_c on I_{sd}. Some authors further impose the condition of intercept convergence for different V_{gs}, which requires that both μ_{FET} and R_c are both independent of σ, another unrealistic assumption.

Various injection models for the contact and the SCLC conduction model for the contact region intrinsically produce nonlinear current–voltage (IV) characteristics and hence nonlinear R_c. For in-plane configurations, it is further known that R_c decreases with increasing σ because of narrowing of the depletion width at the contact [18], while for staggered configurations, R_c may be expected to decrease with increasing σ because of carrier back-diffusion into the contact region to improve injection. Recent work has found that the diffusion tail can contribute to a significant ohmic current in diodes [19]. μ_{FET} may also have a dependence on σ [20]. Thus it is more appropriate to characterize R_c at constant (I_{sd}, σ).

Another key feature of early work is their obsession with R_c itself. Although R_c is an important device parameter, it is not fundamental, but depends on device dimensions and geometry. For the staggered configuration, this includes the intervening semiconductor film thickness t, electrode length L_e, current transfer length L_T, sheet resistance S of the channel extended over (or under) the contact region, and the specific contact resistance $r_{c,i}$ of the