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Local charge accumulation and trapping in grain boundaries of pentacene thin film transistors

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ABSTRACT

We present a comprehensive Kelvin probe force microscopy study of grain boundaries in pentacene transistors with different film thicknesses in combination with current–voltage measurements and 3D electrostatics simulations. It is found that in pentacene films thinner than approximately 30 nm, holes are accumulated in the grain boundaries due to negative trapped charge at the SiO_2–pentacene interface. On the other hand, in thicker films we observe hole depletion near the boundaries mainly due to positive charge trapping in the grain boundaries. The results are discussed in view of their effect on pentacene thin film transistors performance.

1. Introduction

The nature of grain boundaries (GBs) and their role in the charge transport in organic materials in general, and in pentacene in particular is of large interest in recent years. Horowitz and Hajlaoui [1] have shown that the carrier mobility increases with grain size in oligothiophene thin film transistors. Their model suggested that the charge transport is limited by trapping and thermal release at localized states located at the GBs. Other works also suggested that the main bottleneck for the charge transport in organic devices is due to potential barriers both in the GBs, and inside the grains [2–7]. The above works have used macroscopic measurements combined with simulations to study the GBs influence on the device characteristics. It is well known that in organic thin film transistors the current flows very close (few nm) to the gate dielectric interface, which makes the correlation between this accumulation current and the GBs properties extremely difficult.

Puntambekar et al. [8] have used Kelvin probe force microscopy (KPFM) to measure the GBs potential barriers in pentacene thin films (3–5 nm). They have found that the potential drop in the GBs is around 5–10 mV which is an indication of negative trapped charge at the GBs. They also observed that the surface-potential variations within the grains are comparable to the drops at the GBs making it ambiguous whether the GBs poses bottlenecks to hole transport. Wang et al. [9] also argued that the channel mobility and threshold voltage are limited by charged traps in the channel, most of which are not located in the grain boundaries but at the organic/insulating layer interface. Nakamura et al. [10] have shown that the GBs are not always a limiting factor for the carrier mobility, although the mobility had a correlation with the average grain size. Tello et al. [11] have also used KPFM to measure the surface potential in pentacene transistors under bias, and its correlation with the film morphology. They have found that most of the applied drain–source bias drops across a single well-defined grain boundary, which consequently acts as the bottleneck for charge transport. However, these features were scarce, indicating that there is generally sufficient connectivity through the GBs to transport the current.

The above studies indicate that the GBs role in pentacene charge carrier transport and their effect on the device

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performance is not well understood. This is partially due to the lack of simulations combined with local GBs electronic measurements that can quantitatively reveal the effect of the GBs. We present here a comprehensive KPFM study of pentacene thin film organic field effect transistors (OFETs) with different film thicknesses combined with *i–V* measurements and 3D electrostatic simulations in order to reveal and quantify the GBs role on the device characteristics. We distinguish between two different charge trapping regions: the first is the SiO_2–pentacene interface where electrons are trapped, and the second is in the GBs that trap holes (the majority carriers). It is found that the bottom interface charge determines the GBs surface potential in thin layers, while the GBs trapped charge does it in thick layers. The results are discussed in view of their effect on pentacene thin film transistors performance.

2. Experimental

A heavily doped *n*-Si (1 0 0) wafer was used as the substrate and the gate electrode, and thermally oxidized SiO_2 (300 nm) served as the gate dielectric. The pentacene layer was deposited by using the molecular-beam deposition method [12] at a base pressure of 4×10^{-10} Torr and at a growth rate of 0.2 nm min^{-1} with a substrate temperature of 60 °C. The channel width and length of the pentacene transistor were 5 mm and 20 μm, respectively. The source and drain gold electrodes of pentacene TFT were deposited on the pentacene film in vacuum. Four transistors with pentacene layers in thickness of 100, 30, 10 and 5 nm were prepared and transferred to glove box where both the KPFM and electrical measurements were carried out. The KPFM measurements were conducted using a *Dimension 3100* atomic force microscopy (AFM) system in a controlled nitrogen environment glove box (less than ~5 ppm H_2O), in the lift mode where the first scan is a tapping mode topography measurement and in the second scan the tip is raised above the topography trajectory ~5 nm and measures the CPD.

3. Results and discussion

3.1. Thin pentacene layers

Fig. 1 shows topography (top row (a, d and g) and CPD images (second row (b, e and h) for 30, 10 and 5 nm thick pentacene transistors biased above the threshold voltage ($V_g = 0$), respectively. The measured CPD represents the difference between the tip work function (Φ_t) and sample work function (Φ_s) defined as:

$$\mathrm{CPD} = -\frac{1}{q}(\Phi_t - \Phi_s) \quad (1)$$

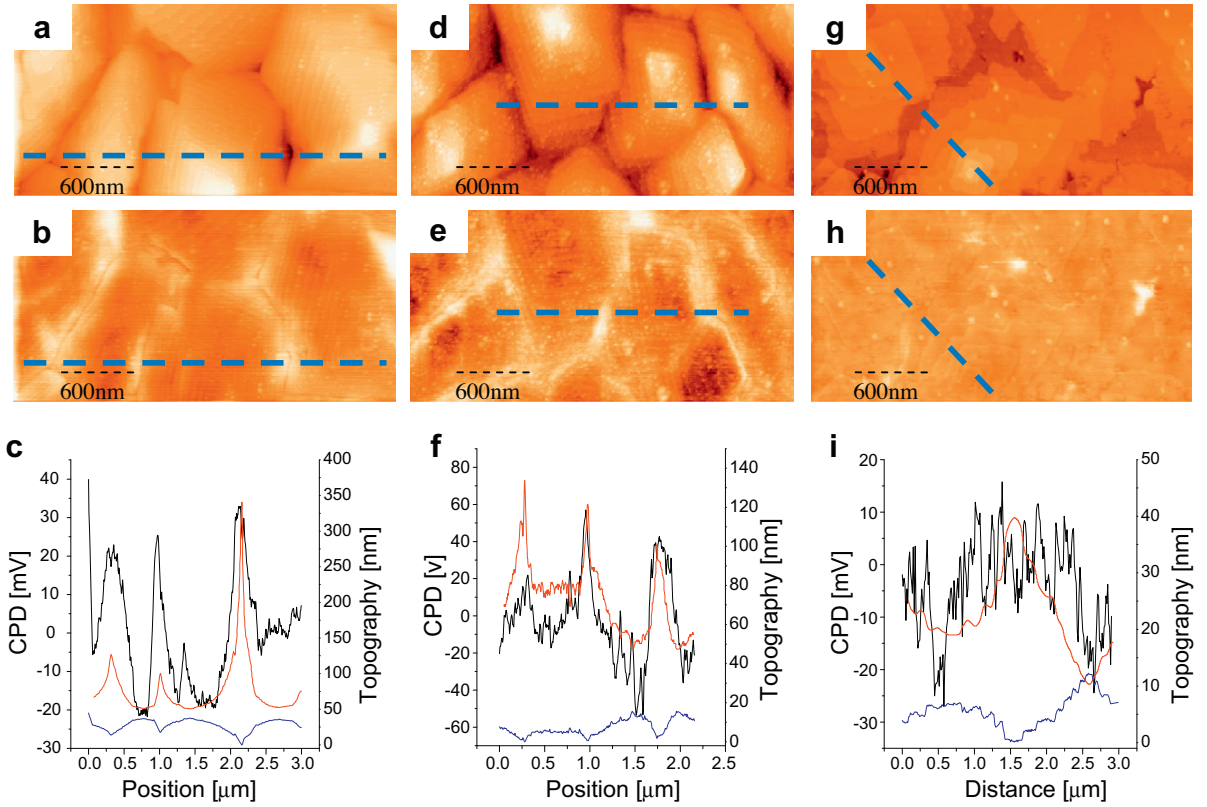

Fig. 1. (a, d and g) Topography of 30, 10 and 5 nm thick pentacene films, respectively. (b, e and h) CPD measurement of 30, 10 and 5 nm thick pentacene film respectively. (c, f and i) lines scans of the calculated and measured CPD of 30, 10 and 5 nm thick pentacene films, respectively. Black line represents the measured CPD, red line the calculated CPD and the blue line represents the measured topography. All the images were measured at $V_g = 0$. (For interpretation of the references in colour in this figure legend, the reader is referred to the web version of this article.)