



Complementary organic thin film transistor circuits fabricated directly on silicone substrates

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ARTICLE INFO

Article history:

Received 30 June 2010

Received in revised form 6 August 2010

Accepted 7 August 2010

Available online 19 August 2010

Keywords:

Organic electronics

Elastomeric substrates

Thin-films

Low temperature process

ABSTRACT

The present work demonstrates organic circuits on a new class of substrate, silicone elastomers. The fabrication method relies on dry, additive processes performed at ultra-low substrate temperature (<100 °C). P-type pentacene and n-type C₆₀ organic thin-film transistors (TFTs) in a bottom gate, top contact architecture are prepared directly on polydimethylsiloxane (PDMS) membranes without any surface pre-treatment. Simple logic elements including complementary inverters and ambipolar transistors patterned on PDMS perform similarly to their counterparts fabricated on substrates thousands times stiffer. The processing options and mechanical compliance of the elastomeric substrate combined with organic device materials open new opportunities for compliant, lightweight, low-power and large area thin-film circuitry.

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1. Introduction

Organic materials have been successfully employed for CMOS-circuitry [1]. Their applications stand in circuits of low complexity such as RF ID tags [2] or in active matrices for displays [3] and electronic skins [4]. Complementary organic electronics have been reported on silicon, polyimide or polyethylene naphthalate (PEN) substrates [5,6]. Non-volatile memories and non-volatile memory transistors for flexible sensor arrays have recently been demonstrated by Sekitani [7,8].

To date, polydimethylsiloxane (PDMS) elastomers are mainly used in microfabricated devices for microfluidics, sensors, MEMS and biomedical applications [9–13]. Their implementation as substrates for microelectronics is a recent evolution. When integrated circuits, first manufactured on and cut into small silicon [14] or plastic [15] platforms, are transferred onto an elastomeric wiring board, the electronic circuit becomes mechanically compliant and even stretchable. The results provide unique electronic systems, which can integrate clothes [16],

conform spherical surfaces [14] and more recently organs [17]. Several strategies for elastic interconnects have been developed and patterned directly onto the elastomeric substrates [14,18–21]. We now propose to also fabricate the electronic circuits directly onto PDMS employing organic small molecules semiconductors. The device process flow is straightforward [22] and compatible with organic thin-film electronics manufacturing.

2. Experimental

PDMS substrates of 1 mm thickness are prepared by casting polydimethylsiloxane (PDMS, Sylgard 184, Dow Corning) in a 10:1 mixing ratio into Petri dishes and curing at 65 °C for 24 h. Alternatively 1 mm thick PDMS membranes (Speciality Manufacturing Inc., MI, USA) are leached for 48 h in isopropanol alcohol followed by blow-drying with nitrogen. A bilayer of 5 nm/50 nm thick Chromium/Gold films is thermally evaporated (rate ~0.1 Å/s) to form the transistor bottom gate electrode. The gate dielectric is formed by vapour deposition of 600 nm thick poly-para-xylylene (Parylene C) film with a capacitance of 4.6 μF/cm² using a Labcoater 2010 (Speciality Coating Systems, UK). Organic semiconductor films of 50 nm

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pentacene (Sigma Aldrich, 98% purity) (p-type) and C₆₀ (MER Corp., 99% purity) (n-type) respectively are evaporated with a rate of $r = 0.4 \text{ Å/s}$, followed by 30 nm of gold to form the source and drain electrodes for the top contacts. Pentacene and C₆₀ TFTs have identical channels with $W/L = 3000 \text{ μm}/200 \text{ μm} = 15$. Complementary organic inverters are further prepared by patterning adjacent p-type and n-type transistor channels. Fig. 1a presents 18 complementary inverters on a transparent 1 mm thick PDMS substrate. Each pair of TFTs shares a common 1 mm gate electrode. The n-type and p-type devices are clearly distinguished from their resulting multilayer colour (Fig. 1b). Fig. 1c shows the schematic view of the inverter. For ambipolar TFTs, the semiconductor layer is formed by evaporating a 50 nm thick pentacene film on a 50 nm thick C₆₀ film (C₆₀/pentacene device) or vice versa (pentacene/C₆₀ device). Channel dimensions for ambipolar TFTs are $W/L = 3000 \text{ μm}/150 \text{ μm} = 20$. Electrodes and the semiconductor layer are patterned through stainless steel shadow masks; the gate dielectric deposited through a PDMS shadow mask. The devices are not annealed.

AFM micrographs of the topography of the thin films on PDMS are obtained using a Pico Plus AFM system (Molecular Imaging) and an NSC360Al cantilever (MikroMasch) with a 1.75 N/m force constant.

TFTs and inverter circuits are characterised in a nitrogen environment using an HP4155 semiconductor parameter analyser.

3. Results and discussion

Fig. 2 summarizes the electrical response of n-type, p-type TFTs and complementary inverters on PDMS. The transfer and $I(V)$ characteristics of a p-channel pentacene TFT on PDMS are shown in Fig. 2a and b. The TFT channel is 3000 μm wide and 200 μm long ($W/L = 15$). The off state current is below 5 nA and the on/off ratio is 10^4 for $V_{GS} \in [-60 \text{ V}; 10 \text{ V}]$. Low leakage gate current is maintained during linear and saturation TFT operation with $I_{GS} < 1 \text{ nA}$. The threshold voltage is -4 V , and carrier mobility in the saturation regime is $0.16 \text{ cm}^2/\text{V s}$. Symmetric results are obtained for the n-type C₆₀ TFT on PDMS (Fig. 2c and d) with equal channel dimensions ($W/L = 15$). Saturation electron mobility and threshold voltage are measured

to be $0.16 \text{ cm}^2/\text{V s}$ and 12 V , respectively. On current at $V_{DS} = 60 \text{ V}$ is 10 μA . Both n-type and p-type TFTs show negligible hysteresis suggesting good gate stability.

C₆₀ and pentacene TFTs are then integrated into complementary inverters (Fig. 1). Fig. 2e shows the transfer curves of an inverter with equally sized n- and p-type channels ($W/L = 3000 \text{ μm}/200 \text{ μm}$) and for supply voltages V_{DD} of 40, 50 and 60 V. The gate is common to both transistors and is the circuit input node V_{in} . The circuit exhibits sharp switching at nearly $V_{DD}/2$. In the off state ($V_{in} = 0 \text{ V}$), V_{out} matches V_{DD} . Voltage gains as high as 21 are recorded from the inverter. This confirms that both transistors have matching performance (Fig. 2f).

Small tensile flexion (bending radius of 6.5 cm) is then applied to the inverters on PDMS. The circuits remain functional inverters after one bending cycle but their performance degrades quickly with further bending. This is expected because the TFT stack is sitting on top of the PDMS membrane without any encapsulation, i.e. away from the mechanical neutral plane, where the tensile strain is about one percent [23].

Ambipolar transistors and inverters based on heterojunctions of pentacene/C₆₀ or C₆₀/pentacene semiconductor films are prepared as an alternative to complementary TFT inverters. Fig. 3a and d show the transfer characteristics for transistors with pentacene/C₆₀ or C₆₀/pentacene semiconductor channels for V_{DS} at 10 V and 60 V. Their channel is 3000 μm wide and 150 μm long ($W/L = 20$). Both devices exhibit a typical ambipolar response with V-shaped transfer curves. On currents for both device configurations are in the micro ampere range, and gate leakage currents are below 10 nA. In the electron accumulation mode, the pentacene/C₆₀ device has a threshold voltage $V_{Th,n}$ of 40 V and yields a saturation electron mobility of $0.12 \text{ cm}^2/\text{V s}$, close to that of the C₆₀ TFT (Fig. 2c). In the hole accumulation mode, the device's threshold voltage $V_{Th,p}$ is -30 V and the corresponding hole mobility is low, $3 \times 10^{-2} \text{ cm}^2/\text{V s}$. The C₆₀/pentacene transistor presents poorer performance with electron mobility of $0.02 \text{ cm}^2/\text{V s}$ and $V_{Th,n} = 12 \text{ V}$, and hole mobility of $\sim 6.5 \times 10^{-3} \text{ cm}^2/\text{V s}$ and $V_{Th,p} = -40 \text{ V}$.

The obtained mobilities for either of our ambipolar device configurations are higher than those reported for similar devices fabricated on Si/SiO₂ or Mylar substrates

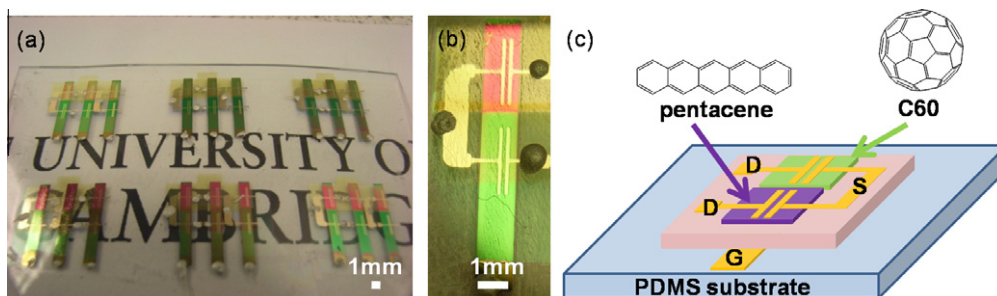


Fig. 1. (a) Photograph of an array of complementary organic inverters on 1 mm thick transparent PDMS. (b) Photograph of a complementary organic inverter prepared on PDMS. The n-type C₆₀ transistor is the top (pink) device; the p-type pentacene transistor is the bottom (green) device. (c) Schematic view of the complementary inverter stack directly prepared on PDMS. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

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