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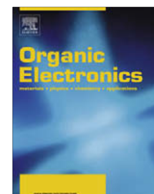

Bottom gate organic thin-film transistors fabricated by ultraviolet transfer embossing with improved device performance

Shi Jingsheng, Mary B. Chan-Park, Chang Ming Li *

School of Chemical and Biomedical Engineering, Nanyang Technological University, 70 Nanyang Drive, Singapore 637457, Singapore

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ABSTRACT

Ultraviolet transfer embossing is optimized to fabricate bottom gate organic thin-film transistors (OTFTs) on flexible plastic substrates, achieving significant improved device performance (μ = 0.01–0.02cm^2/Vs; on/off ratio = 10^4) compared with the top gate OTFTs made previously by the same method (μ = 0.001–0.002 cm^2/Vs; on/off ratio = 10^2). The performance improvement can be ascribed to the reduced roughness of the dielectric-semiconductor interface (R_{rms} = 0.852 nm) and thermally cross-linked PVP dielectric which leads to reduced gate leakage current and transistor off current in the bottom-gated configuration. This technique brings an alternative great opportunity to the high-volume production of economic printable large-area OTFT-based flexible electronics and sensors.

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1. Introduction

Organic thin-film transistors (OTFTs) are receiving increasing interest in the area of printed low-cost and large-area electronics on flexible substrates for applications such as electronic paper, solar panels and flexible sensors [1–3]. To lower the cost of organic electronics, it is important to develop fabrication processes that do not rely on clean room and that are compatible with solution processable dielectric materials and organic semiconductors [4]. Cold welding methods, both subtractive and additive, developed by Forrest's group [1,5,6] are capable to transfer metallic patterns on submicrometer scale by applying high pressure to form metallic bonds at the conformal contact area. In the additive cold welding method, a strike layer for facilitating the bonding process requires a gentle etching or simple sputtering process to be removed. Inkjet printing is an alternative technique to photolithography that has recently reached submicron scale resolution [7]; this process, however, requires a chemically modified ink to fabricate ultra-hydrophobic electrodes and post-printing sintering at a high temperature to increase the conductivity of the electrodes. Screen printing and micro contact printing (μCP) have been actively investigated by different research groups [8], but these techniques are limited to low resolution of ~20 μm. Nanotransfer printing (nTP), developed by rogers' research group as advances of

* Corresponding author. Tel./fax: +65 67904485.
E-mail address: ECMLi@ntu.edu.sg (C.M. Li).

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μCP, offers a better resolution (∼100 nm) comparing to μCP [9,10]. The process utilizes the surface chemistry or noncovalent forces between the receiving surface and transferred metal to form the source and drain electrodes in OTFTs [11,12].

Our lab has previously demonstrated a fast and efficient OTFT fabrication process employing ultraviolet (UV) transfer embossing at room temperature with a resolution (∼2 μm) comparable to lithography process [13]. UV transfer embossing is fast, does not require clean room and can achieve small micron-resolution. The embossing template fabrication itself does require clean fabrication conditions, but once it is made, it may be used repeatedly to produce OTFTs under less stringent conditions. However, our previous top gate devices, regardless of using P3HT or poly(3,3‴-didodecyl quaterthiophene) (PQT-12) (see Supplementary material) as organic semiconductors, have relatively low device performance of mobility (μ) of 0.001–0.002 cm^2/Vs and on/off ratio of 10^2 [13]. The poor performance is attributed principally to the roughness between the PVP dielectric and the semiconductor; this is propagated from the relatively rough PET substrate surface through the thin semiconductor film. The high roughness at the dielectric-semiconductor interface significantly perturbs the structure of the semiconductor and forms many electron traps. Further, the top-gated configuration, which requires deposition of the organic semiconductor prior to deposition of the poly(4-vinylphenol) (PVP) dielectric, prevents thermal cross-linking of the dielectric since that would damage the underlying semiconductor (the typical cross-link temperature for PVP is above 150 °C, which would degrade the semiconductor [14]), with the consequence of high leakage current through the dielectric layer.

In this letter we report our optimization of the UV transfer embossing process by fabricating bottom gate devices with a resolution of ∼2 μm which exhibit much improved device performance. Bottom gate devices allow deposition of PVP dielectric before semiconductor deposition. Fig. 1 shows a schematic illustration of the fabrication process for bottom gate devices by our UV transfer embossing process.

2. Experimental

The UV embossing resin was a mixture of epoxy bisphenol-A diacrylate (Ebecryl 600), dipropylene glycol diacrylate (SR 508) and trimethylolpropane triacrylate (SR 351) with weight ratio of 12:5:3 diluted (50 wt%) in isobutylmethylketone (IBMK). Ebecryl 600 was supplied by UCB chemicals and SR 508 and SR 351 were supplied by Sartomer. Our UV resin mixture offers a fast curing response, good adhesion and superior cured film strength. This formulation was chosen also because the contact between UV resin and PVP thin-film was good enough for the deposition of UV resin on PVP via spin-coating. PVP and methylated poly(melamine-co-formaldehyde) (MPMF, used as PVP cross-linking agent) with weight ratio of 4:1 were dissolved in dimethyl formamide (DMF) to give a 8 wt% solu-

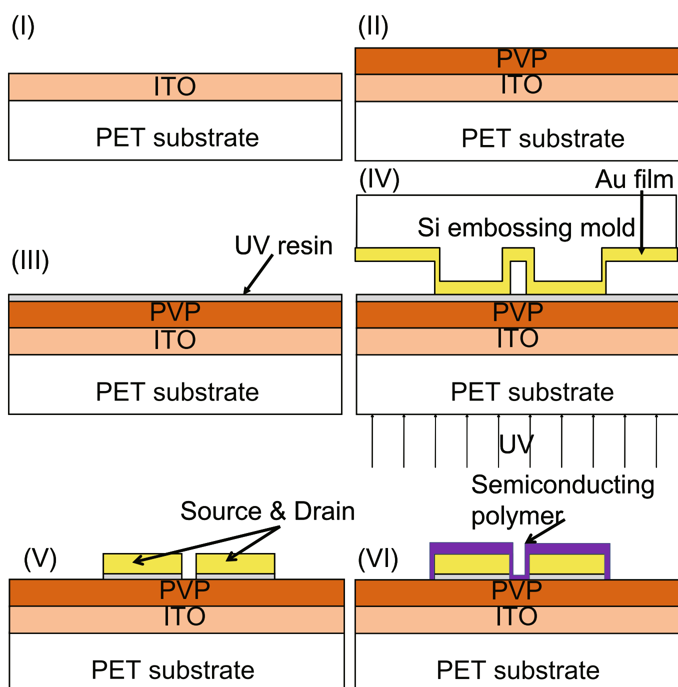

Fig. 1. Schematic illustration of the UV transfer embossing process in fabrication of bottom gate devices: (I) ITO coated PET films are cleaned in detergent, (II) PVP with MPMF is spin-coated on top of ITO and cross-linked in an oven followed with O_2 plasma treatment, (III) UV resin is spin-coated on PVP, (IV) Si embossing mold and UV resin coated substrate are brought into contact and exposed to UV light, (V) source and drain electrodes are transferred onto PVP after demolding and (VI) semiconducting polymer is drop-coated to complete device fabrication.

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