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Origin of bias stress induced instability of contact resistance in organic thin film transistors

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ABSTRACT

We report a study on the contact resistance instability induced by the bias stress in staggered pentacene thin film transistors, combining the bias stress measurements with the transfer line method. The contact resistance is increasing with the stress time, and two device parameters are found to contribute to this contact resistance instability: one is the threshold voltage increase due to the charge trapping in the charge accumulation layer; the other is the effective contact length increase due to the charge trapping in the pentacene bulk in the contact region. The gold contact shows lower contact resistance stability compared with the copper contact, which is ascribed to higher density of the deep trap states at the gold contact. This work suggests that the time-dependent charge trapping is responsible for the bias stress effect in organic thin film transistors.

1. Introduction

Significant efforts and progress have been made towards diverse applications of organic thin film transistors (OTFTs) [1–3], covering the fields of flat-panel displays, radio-frequency identification tags, chemical and biological sensing, etc. For all practical applications, operation stability of OTFTs is critically important, and thus the typically strong bias stress effect in OTFTs [4–8] must be effectively suppressed. The bias stress effect refers to the drain current (I_D) instability of OTFTs with prolonged operation time, and it is well documented that this effect stems from the threshold voltage (V_T) shift accompanied with approximately unchanged field effect mobility (μ_{FE}) [4–8]. However, there are experimental evidences [8,9] revealing that not only the V_T shift in the channel region, but also the contact resistance (R_C) change in the contact region, are responsible for the bias stress induced I_D instability. In the linear regime, I_D can be expressed as [8]

$$I_D(t) = \frac{V_{DS}}{R_{ch}(t) + R_C(t)} = \frac{V_{DS}}{\frac{L}{W\mu_{FE}C_i[V_{GS}-V_{T0}-\Delta V_T(t)]} + R_{C0} + \Delta R_C(t)} \quad (1)$$

where t is the stress time, R_{ch} is the channel resistance, L and W are the channel length and channel width, respectively, C_i is the insulating layer capacitance per unit area, V_{DS} and V_{GS} are the drain bias and gate bias, respectively, $\Delta V_T(t)$ is the V_T shift at t with respect to initial V_{T0}, and $\Delta R_C(t)$ is the R_C change at t with respect to initial R_{C0}. Although the microscopic mechanism of ΔV_T in OTFTs has been extensively investigated [4], the origin of ΔR_C under bias stress condition remains unclear. This issue is of great importance for both fundamental understanding on the bias stress effect and practical approach to highly stable OTFTs.

A precise measurement and a comprehensive description of R_C are the prerequisites to elucidate bias stress induced ΔR_C in OTFTs. Our previous works [10,11] report a crowding current model, which can well interpret the R_C behavior at different V_{GS} and temperature (T). This model concerns the fact that the local electric field

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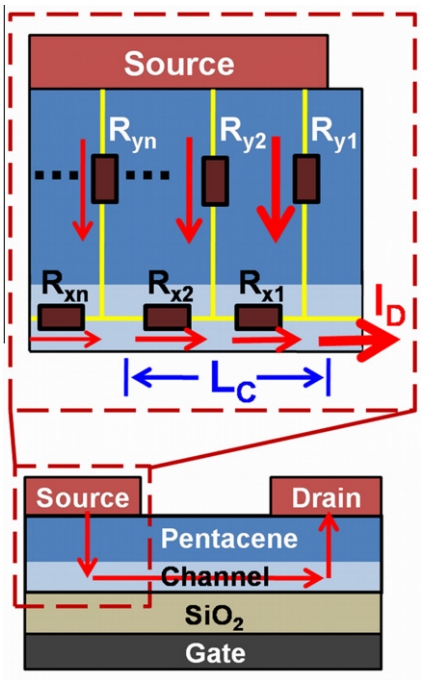

Fig. 1. Schematics of an equivalent circuit at source contact in a staggered OTFT, where charge accumulation layer is shown at vicinity above dielectric layer. Current crowding behavior and effective contact length are illustrated.

distribution in the contact region of OTFTs is not spatially uniform, and thus R_C is the total resistance of an equivalent circuit which can simulate the current flow through the contact region. Fig. 1 shows the equivalent circuit for the crowding current model in a staggered OTFT (top contact with bottom gate), where R_x and R_y are the local accumulation layer resistance in the horizontal direction and local bulk resistance in the vertical direction, respectively. The deduced expression of R_C has the same form as R_{ch}, i.e. [10,12]

$$R_C = \frac{L_C}{W\mu_{FE}C_i(V_{GS} - V_T)} \tag{2}$$

where L_C is the effective contact length referring to the equivalent extended L due to the existence of R_C. We measured ΔR_C under bias stress condition, and observed a continuous increase of both V_T and L_C with t. The observations indicate that the bias stress induced R_C instability stems from the time-dependent charge trapping, which occurs both in the charge accumulation layer and in the organic bulk in the contact region. The systematical comparison between the gold (Au) and copper (Cu) contacts suggests the charge trap distribution in the contact region having a great influence on the R_C instability.

2. Experimental

The pentacene-based OTFTs were fabricated on the heavily doped silicon (Si) substrates with 200-nm-thick thermal oxide (SiO_2) layers (University Wafer). After

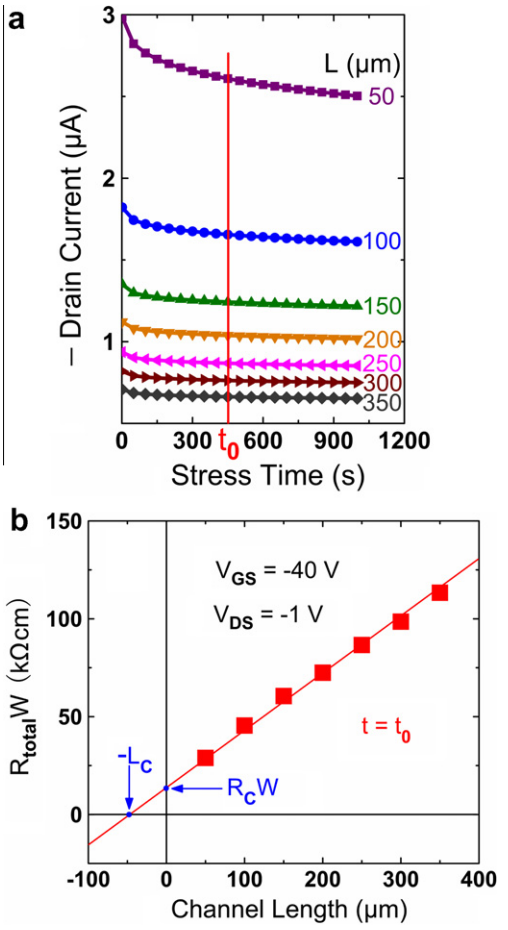

Fig. 2. (a) Drain current vs stress time in a set of pentacene-based OTFTs (Au contact) with varied channel lengths. (b) Transfer line method plot (normalized device total resistance vs channel length) of a set of pentacene-based OTFTs (Au contact) at a particular time point marked in (a), by which contact resistance and effective contact length can be precisely extracted. All TLM plots at different time points show good linearity, indicating that there is no channel length dependence of the threshold voltage shift.

standard cleaning, the substrates were precoated with a self-assembling monolayer of β-phenethyltrichlorosilane (TCI, immersed in β-phenethyltrichlorosilane solution for 6 h in a glove box). The pentacene (TCI, purified with temperature gradient sublimation) films with 40 nm thickness were subsequently deposited in high vacuum about 5×10^{-5} Pa, where the deposition rate and substrate temperature were kept at about 0.1 Å/s and 70 °C, respectively. Eventually, a set of OTFTs, having an identical W = 750 μm and varied L = 50–350 μm with 50 μm interval [8], were defined by depositing Au or Cu top electrodes (electrode length 100 μm, thermal evaporation through a shadow mask).

The bias stress measurements were carried out at room temperature in a high vacuum (about 1×10^{-4} Pa) probe station. After a quick transfer characteristics scan at t = 0 s, I_D at ON state (V_{DS} = −1 V, V_{GS} = −40 V) was continuously measured for 1000 s, followed by another quick transfer characteristics scan at t = 1000 s. As an example, the initial