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# High mobility multibit nonvolatile memory elements based organic field effect transistors with large hysteresis

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A B S T R A C T

High mobility multibit nonvolatile memory elements based on organic field effect transistors with a thin layer of polyquinoline (PQ) were reported. The devices show a high mobility of 1.5 $cm^2 V^{-1} s^{-1}$ in the saturation region which is among the best reported for nonvolatile organic memory transistors. The multibit nonvolatile memory elements can be operated at voltage less than 100 V with good stability under continuous operation condition and show long retention time. The different initial scanning positive gate voltages to −100 V result in several ON states, while the scanning gate voltage from −100 V to positive voltage leads to same OFF state. The charge trapping model of electrons into the PQ layer was used to explain the origin of the memory properties.



## 1. Introduction

Organic memory elements have attracted significant interest recently due to the widespread use of portable electronic devices and its unique advantages, such as low-cost, light-weight and good compatibility to plastic or transparent substrates [1–8]. Among them, nonvolatile organic memory transistors (NOMTs) are especially desirable because of its non-destructive read-out, complementary metal oxide semiconductor architectural compatibility, and single transistor application. Since the first report by Remiens et al., [1] enormous efforts have been devoted to improve the performance of simple device structure NOMTs [9–26]. In order to meet the demands for increased data storage capacity, multi-bit memory devices (i.e., memory devices capable of storing at least 2-bit data per constituent memory cells) have been explored to replace single-bit memory devices because of the limitation of the scaling methods [27]. Guo et al. reported the first light-assisted multibit NOMT device based on pentacene/copper phthalocyaine with a polystyrene or poly(methyl methacrylate) as a modified dielectric layer [28]. However, the multibit memory devices do not show excellent field-effect performance and multibit storage ability, exhibiting a low mobility of 0.5 $cm^2 V^{-1} s^{-1}$ for pentacene and two bits storage in a single device. In addition, the devices also need an additional light source to accomplish multibit memory, which will cost more power. This may also cause photo-oxidative degradation of the organic semiconductor. All these impede the devices to be used for practical applications. Marcus et al. also reported a single wall carbon nanotube-based FET memory element with $HfO_2$ as a gate dielectric with large hysteresis due to charge-trapping of $HfO_2$ [29]. Wang et al. have successfully controlled the threshold voltage by changing the starting gate voltage of transfer curves [30]. Herein, we will explore the feasibility of using gate voltage to control the charge trapping between the dielectric and the organic semiconductor (pentacene) to create large hysteresis for realizing multibit NOMTs. Polyquinoline (PQ) is a commercial dielectric material with good thin film processibility, excellent thermal stability, and low moisture absorption [31–33]. More interestingly, the large difference of electron injection barrier between PQ and dielectric layer (such as $SiO_2$) will allow PQ to be used as a charge trapping material between organic semiconductor and dielectric to enhance both the field-effect performance and the memory effect. To this end, a thin layer of PQ was used as the charge-trapping layer to modify the $SiO_2$ dielectric. The pentacene-based OFETs were fabricated. Pentacene is a highly conjugated polycyclic aromatic

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hydrocarbon, which has been widely studied in OFETs due to its good semiconducting behavior. The mobilities of pentacene-based OFETs have been improved from 0.001 to 3 $cm^2\ V^{-1}\ s^{-1}$ by either using different deposition methods or different gate dielectric layer [34,35]. The transfer curves of pentacene-based OFETs with the PQ modified layer show large hysteresis windows, which could be controlled by the starting gate voltage ($V_{GS}$). This will demonstrate the multibit nonvolatile memory elements with several ON states. The memory elements can work at voltage lower than 100 V with good stability under continuous operation and long retention time. The hysteresis comes from the modulation of the gate field by the trapped charges in the thin PQ layer.

## 2. Results and discussion

The cross-sectional view of the fabricated device structure and molecular structure of PQ are shown in Fig. 1a. The device fabrication is shown in the Experimental Section. Fig. 1b shows the output characteristics of the devices with 20 nm PQ layer that featuring good *p*-type FET behaviours. The good fitting of the current-voltage (I–V) curves to the transistor model in linear and saturation regimes are observed. The transfer characteristics of the memory elements are shown in Fig. 1c and d, and all curves were measured from the various starting source-gate voltage ($V_{GS}$) to −100 V in both the forward and reverse directions at a source-drain voltage ($V_{DS}$) of −5 V. Clear clockwise hysteresis characterized by the reversible, positive hysteresis windows ($V_{T,\ hysteresis} = V_{T,\ reverse} - V_{T,\ forward}$) are found for all the sweep ranges and the large shift of threshold voltage during the reverse gate sweep is observed. For the transfer curve with the starting $V_{GS}$ of 100 V, the hysteresis window is about 70 V, which is comparable to that reported for ferroelectric FETs with poly(vinylidene fluoride/trifluoroethylene) ferroelectric copolymer as a gate insulator [12]. With the shift of the starting $V_{GS}$ from 100 V to 0 V, the hysteresis windows decreased to lower than 10 V. The similar phenomena are also observed from $|I_{DS}|^{1/2}$ versus $V_{GS}$ characteristics. A large hysteresis can be observed when the device operated between the depletion mode (normally "ON" at $V_{GS} = 0$) and the enhancement mode (normally "OFF"). Based on the conventional characterization equation in the linear region, the measured values of the typical field-effect mobility and on/off ratio are 0.5 $cm^2\ V^{-1}\ s^{-1}$ and $10^4$, respectively. It is interesting that all these transfer curves are parallel and the calculated mobilities are similar. This result indicates that the starting $V_{GS}$ value does not affect the mobility of the device. Similar hysteresis can also be observed for the transfer curves in the saturation region ($V_{DS} = -100$ V) (Fig. S1), but the hysteresis windows are smaller than those in the linear region. In addition, the ON and OFF currents are all increased while the on/off ratios are kept at $10^4$. The field-effect mobility of the saturation region was calculated to be about 1–1.5 $cm^2\ V^{-1}\ s^{-1}$, which is among the highest value for the reported NOMTs. The high hole mobility of the transistor is due to the good film morphology, high crystalline of pentacene, and the good interface of pentacene/PQ. The good PQ dielectric and pentacene interface also possibly contributes to the high performance of the transistor. The field-effect mobility of the transistor without PQ film in the saturation region was calculated to be 0.1–0.3 $cm^2\ V^{-1}\ s^{-1}$, which is much lower than the one with PQ film. It is well known that the mobility in the linear region is usually lower than the one in the saturation region since the mobility in the linear region (small $V_{DS}$) is more drain-voltage-dependence and the saturation region mobility is expected to be more field-dependent [36]. The small hysteresis in saturation region is because that the small

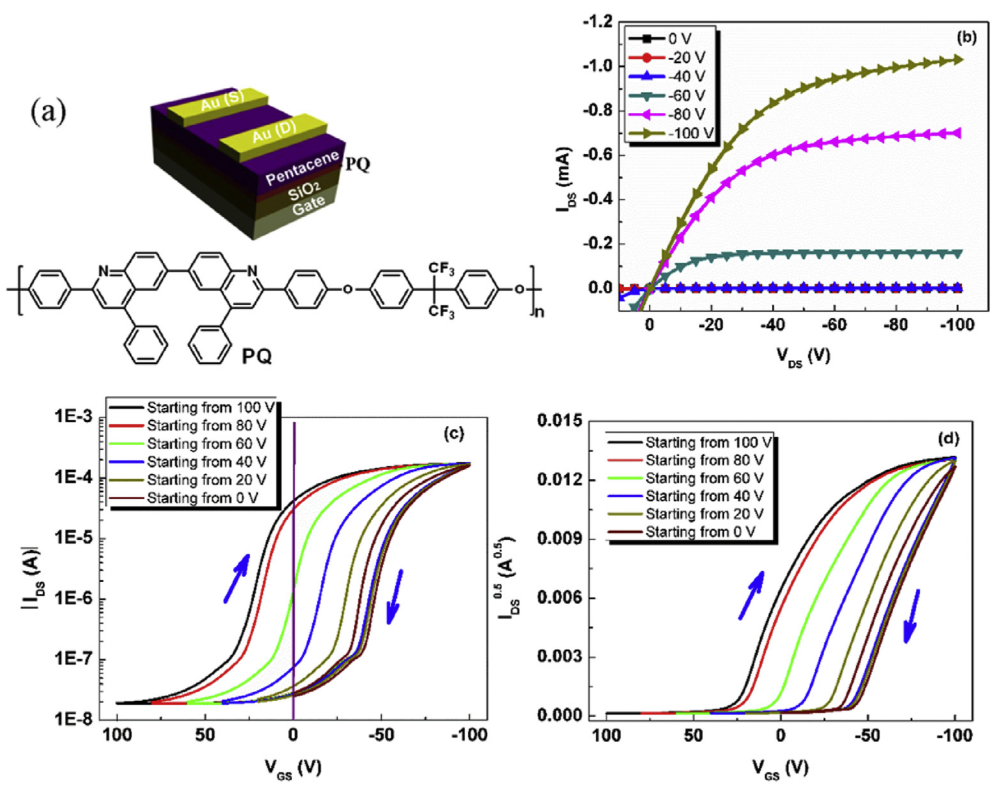


**Fig. 1.** (a) Molecular structure of PQ and the cross-sectional view of NOMTs; (b) Output characteristic of pentacene-based FETs with a 20 nm PQ buffer layer. (c) $|I_{DS}|$ versus $V_{GS}$ and (d) $|I_{DS}|_{1/2}$ versus $V_{GS}$ characteristics of pentacene-based FETs with a 20 nm PQ buffer layer in the linear region ($V_{DS} = -5$ V, W/L = 101). The sweep rate is 0.5 V/s. The forward parts of the transfer curves (from positive voltage to negative voltage) are shifted to negative direction while the backward parts of the transfer curves (from negative voltage to positive voltage) overlap.