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Stable low-voltage organic memory transistors with poly(vinyl alcohol) layers stabilized by vinyl silicon oxide interlayers

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ABSTRACT

Here we report stable transistor-type organic memory devices (TOMDs) with poly(vinyl alcohol) (PVA) gate-insulating memory layers stabilized by vinyl-silicon oxide (VSiO) interlayers that are formed via sol-gel reaction of vinyl triethoxysilane (VTES). The thickness of the VSiO interlayers, which are placed between the PVA layers and the poly(3-hexylthiophene) (P3HT) channel layers, was varied up to 250 nm. In order to investigate the thermal stability, all devices were thermally treated at 150 °C for 30 min. The transistor performance and hysteresis characteristics were greatly improved for the PVA-TOMDs with the VSiO interlayers after thermal treatment, whereas the PVA-TOMD without the VSiO interlayer was severely degraded after thermal treatment. In particular, the thermally-treated PVA-TOMD with the 80 nm-thick VSiO interlayer exhibited stable low-voltage driving and outstanding retention characteristics with >10,000 cycles upon continuous writing-reading-erasing-reading operation.

1. Introduction

Great attention has been paid to organic memory devices (OMDs) due to their potentials as a core component for flexible electronics [1–4]. The advantages of OMDs over conventional inorganic memory devices include flexible/bendable features and easy fabrications of large-area plastic memory modules at low temperatures [3,4] Recently, transistor-type organic memory devices (TOMDs), which are based on the field-effect transistor structures, have been spotlighted because they have both memory and control functions in single device structures [5–14]. In terms of memory functions, most TOMDs are operated by the hysteresis from the gate insulating layers and related geometries which include ferroelectric or high-dielectric polymers, metal nanoparticle/polymer floating gates, polymer energy well structures, etc. [6,10,15–18].

Poly(vinyl alcohol) (PVA), a high-dielectric polymer, has been applied for the gate insulating memory layers in the TOMDs [19–27]. The PVA polymers benefit from environmentally friend wet-coating processes because they are well soluble in water even at high concentrations [28]. The memory function (hysteresis) of PVA is known to be originated from the alignment of hydroxyl groups (OH) leading to the high local dipoles, even though an ionic impurity has been reported to partly affect the hysteresis behavior in the PVA films [22,26,27]. Interestingly, the molecular weight of PVA polymers was found to greatly influence on the performance of TOMDs [27]. In particular, the TOMDs with the PVA layers, which were treated at temperatures lower than 70 °C, exhibited outstanding data retention characteristics featuring >10,000 cycles upon continuous writing-reading-erasing-reading (WRER) operations in our previous report [27]. Considering the typical glass transition temperature of PVA (85 °C), it is assumed that the deformation of the PVA layers by thermal treatment may have a serious influence on the performance of the PVA-TOMDs [29]. However, no study has been so far reported on the effect of thermal treatment on the device performance and data retention characteristics for the PVA-TOMDs, even though the operation stability of memory devices should be guaranteed at 150 °C in addition to the

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typical room temperature stability for commercialization [30,31].

In this work, we demonstrate that the stability of the PVA-TOMDs with the poly(3-hexylthiophene) (P3HT) channel layers could be significantly improved by introducing the vinyl-silicon oxide (VSiO) nanolayers, which are formed via sol-gel processes of vinyl triethoxysilane (VTES) precursors, between the PVA and P3HT layers. The hysteresis characteristics became much better for the PVA-TOMDs with the VSiO interlayers by thermal treatment at 150 °C, whereas the pristine devices without the VSiO interlayers lost hysteresis characteristics by the thermal treatment. In particular, the thermally treated PVA-TOMDs exhibited good memory performances at low voltages (gate voltage = ±3 V; drain voltage = ±1 V) and excellent data retention characteristics (>10,000 cycles) upon continuous WRER operations.

2. Experimental section

2.1. Materials and solutions

PVA (weight-average molecular weight = 9.5 kDa) and VTES (purity = 97%) were purchased from Sigma-Aldrich Co (St Louis, Mo, USA), while P3HT (weight-average molecular weight = 30 kDa, polydispersity index = 1.7, regioregularity = 97%) were supplied from Rieke Metals (Lincoln, NE, USA). The PVA solutions were prepared by dissolving the PVA powders in deionized (DI) water at a solid concentration of 50 mg/ml, while the P3HT solutions were prepared using toluene as a solvent at a concentration of 10 mg/ml. These solutions were subject to vigorous stirring at room temperature. The VSiO precursor solutions were prepared by mixing VTES, DI water (DIW) and acetic acid (AA) (VTES:DIW:AA = 1:1:6 by molar ratio), which were slowly stirred on a hot plate for 24 h at 25 °C (room temperature) for sol-gel process.

2.2. Device fabrication

For the fabrication of devices indium-tin oxide (ITO)-coated glass substrates were patterned to make the ITO stripes as a gate electrode by employing typical photolithography/etching processes. The patterned ITO-glass substrates were cleaned with acetone and isopropyl alcohol and treated under ultraviolet-ozone environment at the UV intensity of 28 mW/cm^2 for 20 min. Next, the PVA solutions were spun on the patterned ITO-glass substrates to make the PVA layers (thickness = 250 nm), followed by soft-baking at 70 °C for 14 h. Then the VSiO precursor layers (thickness = 0, 80, 120, 250 nm) were spin-coated on the PVA layers and soft-baked at 70 °C for 2 h. Finally, the P3HT layers (thickness = 60 nm) were spin-coated on the PVA or VSiO layers, followed by soft-baking at 70 °C for 15 min. These film samples were moved to a vacuum evaporation chamber installed inside an argon-filled glove box system. After the vacuum level of the chamber reached ca. 1x10^{-6} torr, the source/drain electrodes of 10 nm-thick nickel (Ni) and 50 nm-thick aluminum (Al) were deposited on the P3HT layers through a metal shadow mask with the 70 μm-wide metal bridge. The device channel length (L) and width were 70 μm and 3 mm, respectively. One set of devices fabricated on the same day was thermally treated at 150 °C for 30 min inside the argon-filled glove box, while another set was stored in the same glove box without any treatment before measurements.

2.3. Measurements

The transistor and memory performances of devices were measured using a semiconductor parameter analyzer (Keithley 2636B). All measurements were carried out using a sample holder that is filled with argon gas. The data retention characteristics were measured by employing the continuous WRER cycle method, while the write-once-read-many (WORM) test was also performed to examine the repeated reading stability of devices.

3. Results and discussion

As illustrated for the device structure in Fig. 1a, the VSiO interlayers are placed between the PVA and P3HT layers so that they can block the direct contact between the gate insulating memory layers (PVA) and the channel layers (P3HT). Here the VSiO interlayers are considered to have good dimensional stability due to the chemically cross-linked network structures that connect each VTES core part (see Fig. 1b), which may provide high stability during thermal treatment of devices at 150 °C for 30 min. As shown in Fig. 1c, the optical absorbance was gradually increased with the thickness of the VSiO layers in the UV region. However, the presence of the VSiO layers did not change the optical transparency of the resulting films even after thermal treatment (see the inset photograph in Fig. 1c).

The output performance of transistors was first examined according to the thickness of the VSiO interlayers (Fig. 2a). All devices before thermal treatment showed typical p-type transistor behavior because the drain current (I_D) was gradually increased with the negative increase of drain voltage (V_D = 0 V ~ −5 V) and gate voltage (V_G = 0 V ~ −5 V), even though no clear current saturation was measured from the output curves. As the thickness

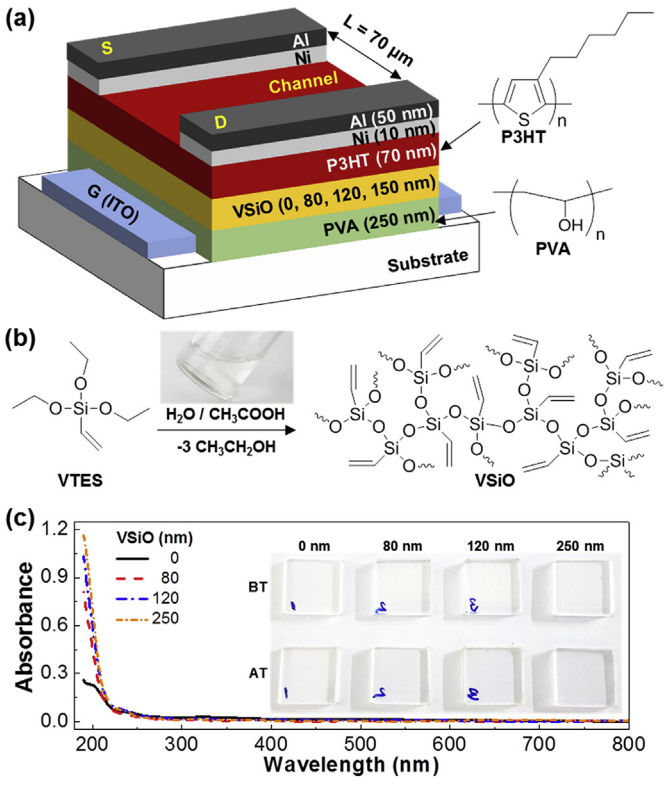

Fig. 1. (a) Illustration for the device structure of the PVA-TOMD with the VSiO interlayer: PVA, P3HT and VSiO denote poly(vinyl alcohol), poly(3-hexylthiophene) and vinyl silicon oxide, respectively. The thickness of PVA and P3HT was 250 nm and 70 nm, respectively, while the thickness of VSiO was varied up to 150 nm. (b) Scheme for the sol-gel reaction of vinyl triethoxysilane (VTES) leading to the VSiO layers. (c) Optical absorption spectra of the PVA/VSiO layers coated on quartz substrates (quartz/PVA/VSiO) according to the thickness of the VSiO layers (Inset: photographs before (BT) and after (AT) thermal treatment at 150 °C for 30 min).