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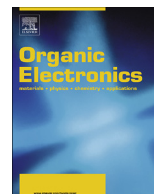

Letter

Low-voltage nonvolatile multi-bit memory fabricated by the patterning and transferring of ferroelectric polymer film

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ABSTRACT

In ferroelectric material, polarization is defined as a volumetric density of dipole moments; therefore, macroscopically many different states of polarizations between positive remanent polarization and negative remanent polarization can be addressable. Simply by controlling the voltage range, multi-states of polarization could be possible. However, for reliable operation of such a multi-bit memory system, all individual states must be completely separated from other states such that only a certain portion of dipoles in a memory device needs to be switched at a certain state. Such a reliable operation would be achieved by spatially separating the switching area in which the individual thickness is different. In this work, it is demonstrated that reliable ferroelectric multi-bit memory could be realized by patterning and transferring ferroelectric polymer film. Also, for low-voltage operation, the highest thickness was designed as 150 nm, which enabled the multi-bit memory to operate within maximal 20 V. Furthermore, a timing diagram, retention and fatigue measurements showed that the fabricated multi-bit memory would be quite promising for emerging organic electronics.

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1. Introduction

Over the last decade, vinylidene fluoride (VDF) – based ferroelectric polymers have received a great deal of attention due to their advantages of superior material properties and process easiness. First, ferroelectric polymer such as poly(vinylidene fluoride–trifluoroethylene), P(VDF–TrFE), is highly insensitive to the environment [1–3], which enables reliable operation of P(VDF–TrFE) so that it can be used with many electronic applications [4–9]. A second important advantage is facility of process. Inorganic ferroelectric materials require high temperature and high vacuum processes for ferroelectricity while ferroelectric polymer needs only annealing at relatively low temperature [10]; therefore, it is adequate for solution process and printing process [11–13]. Mechanical flexibility and optical transparency also make the ferroelectric polymer attractive for emerging applications [14–16]. Using these properties of ferroelectric polymer, in this work, a multi-bit memory device and a new fabrication method to realize it are demonstrated.

Recently, various multi-bit memory devices with ferroelectric polymer have been reported [17–21]. The multi-bit memory devices were realized by controlling the external voltage applied in a ferroelectric capacitor [17–20] and tuning the spatial thickness of ferroelectric film [21]. In general, the structure of a ferroelectric polymer capacitor is described as a scheme shown in Fig. 1a, in which the remanent polarization (P_R) value of the ferroelectric

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capacitor depends on the maximum applied voltage (V_{MAX}) in Fig. 1b, so the P_R–V_{MAX} relationship appears as a solid black-line (f_{origin}) in Fig. 1c. For the case of 2-bit storage multi-bit memory devices, for instance, the two kinds of applied voltage (V_A) values to address each state are required. For simplicity, let us denote the maximum voltage and the middle voltage as V_2 and V_1, respectively. If the thickness of ferroelectric film (t_F) is varied by process tolerance, f_{origin} will move to f^L_{shift} or f^R_{shift}. While the P_2 value for V_2 is almost constant, the P_1 value will be excessively varied by ΔP_1^{origin}, even by a small shift of f_{origin}. The imprint effect [22] and V_A tolerance as well as t_F tolerance will cause the analogous phenomenon. On the other hand, the P_R–V_{MAX} relationship (f_{new}) with a plain near middle state of P_1, as shown in Fig. 1d, will be helpful to avoid the above-mentioned malfunctions in that process, and operation tolerance can be ignored by a tiny variation of ΔP_1^{new}.

Ferroelectric multi-bit memory with a characteristic in Fig. 1d exhibits a hysteresis loop, as shown in Fig. 2a, in which four plains of polarizations are designated as the logic states of 00, 01, 10, and 11, respectively. This hysteresis can be realized by the linear combination of two different hysteresis loops, as depicted in Fig. 2b, which corresponds to two parallel-connected ferroelectric capacitors, as described in Fig. 2c. Assume that C_A capacitor has a coercive voltage of V_{C1}, which is less than V_{C2} in C_B, and initially 11 state is written in the ferroelectric multi-bit memory device. When the applied voltage (V_A) is positioned between $+V_{C1}$ and $+V_{C2}$, the polarization of C_A will be reversed, but C_B operates as ordinary capacitor because V_A smaller than V_{C2} cannot switch the dipoles in C_B. In this case, the stored logic state moves to 01 state. V_A larger than V_{C2} will make the logic state move to 00 from 01. C_A no longer has polarization to offer; as a result, only C_B contributes to the total polarization switching over V_{C2}. Similarly, logic state 10 can also be addressed from a logic state of 00 by applying V_A between $-V_{C1}$ and $-V_{C2}$.

This multi-bit memory scheme fabricated by nanoimprint has been reported, but its operating voltage is quite high because the nanoimprint process could successfully be performed with a thick polymer substrate [21]. Therefore, thin ferroelectric film below the 100-nm-scale is hard to achieve, so this makes the multi-bit memory device operate at higher voltage. In this work, two thicknesses of ferroelectric film will be realized by the pattering and transferring of ferroelectric polymer film, resulting in sub-20 V operation due to a maximum thickness of 150 nm. More details for realization will be given in the following section.

2. Experiment

2.1. Preparation of ferroelectric film

Pellet-type poly(vinylidene fluoride-co-trifluoroethylene) (P(VDF–TrFE)), 75/25 mol%, MSI Sensors Inc.) was purchased and 0.03 g of P(VDF–TrFE) was dissolved in 1 mL of methyl-ethyl-ketone (MEK) (3 wt%) with stirring. To control the thickness of the ferroelectric polymer film (FPF) linearly, spin coating conditions such as spin speed and spin time were fixed to 1500 rpm and 10 s, respectively. Thus, the different thicknesses were achieved by diluting ferroelectric polymer solution with the solvent of MEK. In these conditions, the relationship between film thickness and polymer concentration was 90 nm per 1 wt%. After spin-coating, the FPF was annealed at 130 °C on a hot plate for 1 h to increase the crystalline β-phase. The thickness of FPF was measured using α-step (Dektak 6 M, Veeco Instruments, Inc.).

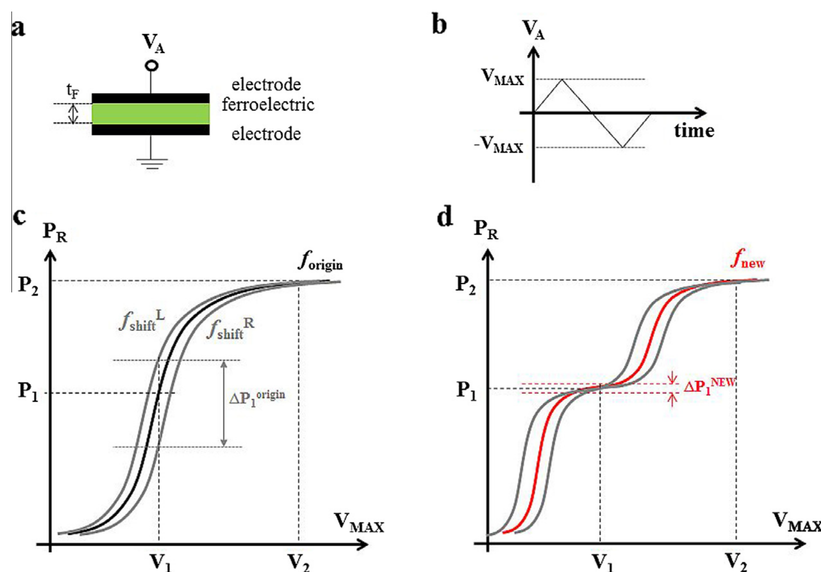

Fig. 1. Requirements for reliable multi-bit memory operation. (a) Schematic of an ordinary ferroelectric capacitor with the structure of electrode/ferroelectric/electrode. (b) Triangular pulse for hysteresis loop measurement. (c) Remanent polarization (P_R)–V_{MAX} relationships for an ordinary ferroelectric capacitor. The two logic states of P_1 and P_2 can be addressable by V_1 and V_2. f_{origin} means the designed properties, f^L_{shift} and f^R_{shift} can be obtained by process tolerance. ΔP_1^{origin} is a variation of P_1 by the shift of f_{origin} (d) remanent polarization (P_R)–V_{MAX} relationships for a proposed ferroelectric multi-bit capacitor; ΔP_1^{new} is a variation of P_1 by the shift of f_{new}.

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