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Solution processable bilayered gate dielectric towards flexible organic thin film transistors

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ABSTRACT

In this study, we have successfully explored the potential of a new bilayer gate dielectric material, composed of Polystyrene (PS), Pluronic P123 Block Copolymer Surfactant (P123) composite thin film and Polyacrylonitrile (PAN) through fabrication of metal insulator metal (MIM) capacitor devices and organic thin film transistors (OTFTs). The conditions for fabrication of PAN and PS-P123 as a bilayer dielectric material are optimized before employing it further as a gate dielectric in OTFTs. Simple solution processable techniques are applied to deposit PAN and PS-P123 as a bilayer dielectric layer on Polyimide (PI) substrates. Contact angle study is further performed to explore the surface property of this bilayer polymer gate dielectric material. This new bilayer dielectric having a k value of 3.7 intermediate to that of PS-P123 composite thin film dielectric ($k \sim 2.8$) and PAN dielectric ($k \sim 5.5$) has successfully acted as a buffer layer by preventing the direct contact between the organic semiconducting layer and high k PAN dielectric. The OTFT devices based on α,ω-dihexylquaterthiophene (DH4T) incorporated with this bilayer dielectric, has demonstrated a hole mobility of 1.37×10^{-2} and on/off current ratio of 10^3 which is one of the good values as reported before. Several bending conditions are applied, to explore the charge carrier hopping mechanism involved in deterioration of electrical properties of these OTFTs. Additionally, the electrical performance of OTFTs, which are exposed to open atmosphere for five days, can be interestingly recovered by means of re-baking them respectively at 90 °C.

1. Introduction

Organic thin film transistors (OTFTs) are one of the widely investigated class of organic electronic devices for their application in future electronic devices. This is because of the numerous merits associated with them such as they are lightweight, bendable, conformable, rugged and easy to fabricate with inexpensive techniques [1]. Transistors based on organic semiconductors are referred to as OTFTs and their configuration is similar to their inorganic counterpart's i.e. Si based transistors. An OTFT device is composed of three main parts: a thin organic semiconductor layer, a dielectric (or insulator), and three electrodes (gate, source and drain). The source and drain electrodes directly contact the semiconductor, whereas the gate electrode is separated from the semiconductor by a dielectric layer. The gate turns the device on and off with an applied voltage and thus controls the current flow (I_{DS}) in the semiconductor between source and drain electrodes. Hence, the

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dielectric layer also plays a critical role in electrical performance of OTFTs. Further, the mobility and threshold voltage of OTFTs in the linear regime are related by the equation [2] below,

$$I_{DS} = \frac{WC_i}{L}\mu_{FE}(V_G - V_{th})V_{DS} \quad (1)$$

where W and L denotes the source–drain width and length, respectively; μ_{FE} is the field effect mobility; C_i is the capacitance per unit area of the insulator, and V_{th} is the threshold voltage. I_{SD} and V_{DS} are the current and voltage bias between source and drain. Thus, the proper choice of the dielectric material having low leakage current and high capacitance is essential for the low operating voltage OTFTs. Exploring new organic semiconductors for their application in OTFTs is one of the most common strategy to enhance the performance of OTFTs [3]. Another innovative idea in this direction is to study the effect of gate dielectric layer on performance of OTFTs [4]. Dielectric surface properties affect the trapped charge densities at the interface between the semiconductor and the gate dielectric, thus it affects the field-effect mobility and the threshold voltage dramatically. Therefore, research on gate dielectric material can open up a way to overcome the major hurdle to some extent coming in the commercialization of OTFTs. Namely, these are their low output current and high operating voltage, as resulting from low charge carrier mobility of the active semiconducting layer as employed respectively in them [5]. For example, Hwang et al. have reported the importance of dielectric layer by employing silk fibroin as a gate dielectric through fabrication of pentacene OTFTs on the flexible poly(ethylene terephthalate) (PET) plastic substrate [6]. The planer structure of the silk fibroin dielectric has allowed the pentacene molecules to self-assemble in the planner form which has resulted in a very high μ_{FE} value of 23.2 $cm^2 V^{-1} s^{-1}$ in the saturation regime and a low operating voltage of −3 V. Hence, the proper choice of dielectric material having good compatibility with the semiconducting layer is also much needed to be explored for optimum performance of OTFTs.

Silicon dioxide (SiO_2) is one of the most common traditional inorganic insulator that has been widely employed as a gate dielectric material in TFTs on commercial scale. Apart from merits, some demerits are also associated with the use of SiO_2 as an insulator. These include high temperature processing (>400 °C), mechanical flexibility and requirements of highly sophisticated laboratories of which are the most common [7]. This has led to the emergence of organic and polymeric dielectric materials for their application in OTFTs. The organic and polymeric materials are able to form high qualified thin films by simple low cost processing methods such as spin coating, ink-jet printing and sol–gel process [8]. Therefore, material scientists are pursuing them over traditional SiO_2 dielectric. Some of the most extensively explored organic polymer dielectrics [9] are poly(methyl methacrylate) (PMMA; $k \approx 3.5$), poly(styrene) (PS; $k \approx 2.6$), poly(4-vinyl chloride) (PVC; $k \approx 4.6$), and cyanoethyl pullulan (CYEPL; $k \approx 18.5$). The dielectric materials can further be divided into two categories based on dielectric (k) value. The high-k dielectrics are dielectrics having a dielectric constant or k-value, higher than that of silicon nitride ($k > 7$) and low-k dielectrics are dielectrics having a dielectric constant, or k-value, lower than that of a silicon dioxide ($k < 3.9$). High performance devices can be achieved by incorporating the low k materials in device system. Recent research studies have found that high k material might lead to electrical degradation of the devices due to the undesired interaction between organic semiconductors (OSCs) and high k dielectric layer [10]. However, low k materials provide benefits of minimum Resistance–Capacitance delay (R–C), cross talk noise and power dissipation [11]. Currently, there have been an increasing demand of reducing the feature size of microelectronics but as device size is decreased Resistance–Capacitance delay increases which is a serious limitation to the scaling down dimension. Hence, replacing the silicon dioxide with a low-k dielectric material of the same thickness can reduce parasitic capacitance which can further enable faster switching speeds and lower heat dissipation.

In this study, we have implemented a strategy of employing low k, PS-P123 buffer layer for high k, PAN gate dielectric through fabrication of OTFTs on the PI flexible substrate to avoid the undesired interaction between high k material and OSC layer. For the OSCs material, a Π – conjugated oligomer semiconductor α,ω-dihexylquaterthiophene (DH4T) was employed due to its easy ability to be deposited by solution process. Further, we have explored that the degraded electrical property of these OTFTs due to their exposure to open atmosphere can be recovered simply by baking them on hot plate. Simple solution processes like spin coating and drop casting has been employed in this study for fabrication of electronic devices in this study. We have also tested reliability and flexibility test of these devices under different bending conditions

2. Experimental section

2.1. Reagents and materials

Polystyrene (PS) (M_w = 54,000) and Pluronic® P123 Block Copolymer Surfactant [water-soluble triblock copolymers of poly(ethy1ene oxide) (PEO) and poly(propy1ene oxide) (PPO)] was procured from Sigma Aldrich and used as received. Polyacrylonitrile (PAN) with M_w 1.5×10^5 was also procured from Sigma Aldrich. The dielectric constant of P123 is 2.8 and dimethylformamide (DMF), chloroform, tetrahydrofuran (THF) solvents were obtained from Alfa Aesar. Chromium shots (Cr, 99.999%, Admat Inc.) 3–5 mm in size, aluminum shots (Al, 99.999%, Admat Inc.) 3–5 mm in size, and gold shots (Au, 99.999%, Admat Inc.) 1–2 mm in size, were purchased from Gredmann Taiwan Ltd. The organic semiconductor (p-type) α,ω-dihexylquaterthiophene (DH4T): M_w = 49,833 was adopted for this research from Sigma Aldrich. DuPont Kapton Polyimide film, 38 μm in thickness from PV9100 series was used as a substrate for fabrication of all devices in this study. All other reagents and solvents were obtained from commercial suppliers and used as such, unless specified. It should be noted that all experiments were performed