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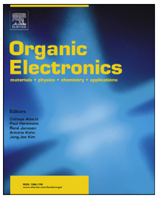

Data retention in organic ferroelectric resistive switches

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ABSTRACT

Solution-processed organic ferroelectric resistive switches could become the long-missing non-volatile memory elements in organic electronic devices. To this end, data retention in these devices should be characterized, understood and controlled. First, it is shown that the measurement protocol can strongly affect the 'apparent' retention time and a suitable protocol is identified. Second, it is shown by experimental and theoretical methods that partial depolarization of the ferroelectric is the major mechanism responsible for imperfect data retention. This depolarization occurs in close vicinity to the semiconductor-ferroelectric interface, is driven by energy minimization and is inherently present in this type of phase-separated polymer blends. Third, a direct relation between data retention and the charge injection barrier height of the resistive switch is demonstrated experimentally and numerically. Tuning the injection barrier height allows to improve retention by many orders of magnitude in time, albeit at the cost of a reduced on/off ratio.

1. Introduction

There is an increasing demand for non-volatile memory elements in organic electronics [1,2]. Solution-processed organic ferroelectric resistive switches have recently been proposed as a very promising practical realization of a non-volatile memory that can be read out non-destructively and is compatible with flexible electronics and large area applications [3,4]. The organic ferroelectric resistive switch consists of a thin film made of a polymeric semiconductor-ferroelectric blend sandwiched between two electrodes. The phase separation in the blend is driven by a spinodal decomposition process which results in sub-micron sized semiconductor domains embedded in an insulating ferroelectric matrix [5–8]. Thus, transport of charge carriers, which is needed for the resistive read out, is possible only via the semiconducting phase. The working principle of the resistive switch relies on a modulation of the barrier for charge injection from the metal electrode into the semiconductor by the polarization charges in the ferroelectric [9,7]. This makes it possible to switch the device between high- and low-resistive states. The non-volatility and bistability of the resistive switch stem from the remnant polarization of the ferroelectric part of the blend.

Data retention is a crucial parameter for memory elements. It is known that the depolarization phenomenon that occurs in the ferroelectric is the major factor that harms the device performance [10]. However, the detailed mechanism of information loss, especially at the local scale, is unknown. Moreover, although there are a number of publications in which data retention of organic resistive switches is studied [11–13], the exact measurement scheme was not always specified. This hampers both comparison between reports and the assessment of the actual relevance for applications.

Here we address the related questions regarding the importance of a well-chosen measurement protocol, the mechanism of the information loss, and ways to mitigate data retention. We show that the data retention is intimately linked to the morphology of the phase-separated polymer blend and is due to polarization loss in a narrow region around the semiconducting domains. From theoretical considerations we show that the polarization in this region is inherently instable. As such, the mechanism governing retention in our devices is fundamentally different from those in ferroelectric-only devices [14,15] and in semiconductor-ferroelectric-metal multilayers [16,17]. Mitigation of this fundamental problem is however possible. We find a direct relation

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between data retention and the charge injection barrier height of the resistive switch which allows to improve retention by many orders of magnitude in time, albeit at the cost of a reduced on/off ratio.

2. Results and discussion

Fig. 1a shows the hysteretic current–voltage (I–V) curve measured on the device fabricated with a P(VDF-TrFE):F8BT 9:1 blend. The contribution from electron transport to the total current is thought to be negligible because of the low electron mobility in F8BT [19] even when the use of Ba as top electrode material warrants a close to ohmic electron injection. A bilayer of 100 nm Au and 1 nm MoOx was chosen as bottom electrode for hole injection. The work-function of this electrode is estimated to be ~5.0 eV [18] because of the presence of MoOx. Since the energy level of the highest occupied molecular orbital (HOMO) of F8BT amounts to 5.9 eV vs. vacuum, the hole injection barrier is of the order of 1 eV. An important advantage of using MoOx is that it was found to prevent the formation of a so-called wetting layer of F8BT – a thin semi-continuous layer of F8BT at the bottom electrode due to a favourable interaction between F8BT and gold [6]. The asymmetry between the positive and negative branches of the I–V curve results from the unequal top and bottom contacts. Without ferroelectric polarization the large charge injection barrier limits hole injection and, therefore, the current in the device is low. However, the injection barrier can be tuned with the assistance of the stray field of the ferroelectric polarization charges [7,9]. The ascending curve in Fig. 1a shows that upon increasing the applied voltage the ferroelectric becomes polarized which consequently lowers the injection barrier, leading to a significant current increase which occurs at around the coercive voltage of +10 V [20]. As the ferroelectric preserves its polarization state when the applied voltage is turned off, the descending part of the I–V curve does not follow the ascending one. Thus the positive part of the I–V sweep demonstrates significant hysteresis behaviour and the device can be programmed to the ON and OFF states. The resistive switch is characterized by the I_{ON}/I_{OFF} ratio of ~10^3, the ratio of the ascending and descending curves, measured at a particular read-out voltage (dashed line in Fig. 1a).

Retention measurements on the same device were done by programming the device to the ON and OFF states and subsequently monitoring the corresponding I_{ON} and I_{OFF} currents over time at the read-out voltage shown in Fig. 1a. It is important to notice that such measurements can be done using at least two different protocols – short-circuit and constant applied voltage respectively. In the former case the read-out voltage is only occasionally applied to the otherwise short circuited device to detect the I_{ON}, I_{OFF} currents. In the latter case the device remains constantly under (read-out) bias. Fig. 1b shows the data retention of the device in Fig. 1a. An important finding is that the same device appears to show significantly better memory characteristics when characterized in constant read voltage mode. This is because the polarization state of the ferroelectric is partially prevented from the depolarization by the applied field. In contrast, in the short-circuit mode the device is left undisturbed. This method is representative for actual operational conditions in non-volatile memory devices and should therefore be preferably used. It is used in the rest of the text.

The reason that the off-state current in Fig. 1a is higher for the constant read voltage protocol (open symbols) than for the short-circuit protocol (closed symbols) is that in the constant read voltage protocol the OFF-state is stabilized by a negative bias (−6 V). When reading at +6 V for comparison with the ON-state current, a small transient ionic contribution results. The same ionic current causes the hysteresis in Fig. 1a. It should be stressed that in all experiments shown herein, the OFF-current is determined by injection and transport in the semiconducting phase and not by leakage through the ferroelectric phase.

In order to understand the underlying mechanism of the information loss the depolarization in the ferroelectric phase of the device was studied using the double-wave method (DWM). In the DWM a sequence of one 'set' and two (identical) 'probe' pulses is applied and the corresponding switching currents are measured [20] (Fig. S1 in SI). The set signal is used to set the desired polarization state of the ferroelectric. The probe pulses are used for studying the prepared ferroelectric polarization. The response to the first probing pulse will contain both the (interesting) switching current and the (undesired) leakage and displacement currents. As the response to the second pulse contains only the latter contributions, these can be subtracted to obtain the switching current. The DWM is more accurate when the switching currents are large compared to the background. This condition is met in reverse bias (Fig. 1a) – the device demonstrates a low current at the negative voltage. Thus the DWM is applied by first setting the memory to the ON state and therefore switches at reverse (negative) bias where the current is low. By knowing the saturated polarization of the ferroelectric the initial polarization state of the device can be retraced. Fig. 2 shows the ascending part of the ferroelectric polarization hysteresis loop measured right after programming the device and after keeping it for 1 day (~10^5 s) at short-circuit

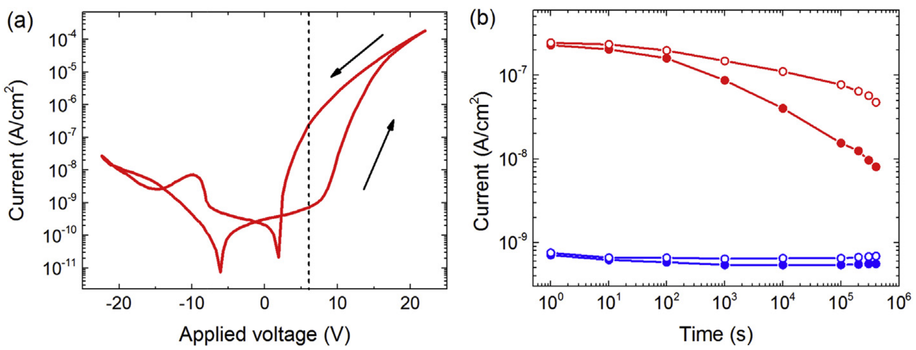

Fig. 1. Electrical and memory characteristics of a ferroelectric memory switch fabricated based on a P(VDF-TrFE):F8BT 9:1 blend with Au/MoOx bottom and Ba/Al top electrodes. (a) Hysteretic current–voltage sweep. Arrows indicate the scan direction, the dashed line at 6 V marks the read-out voltage used in the retention measurements in panel b. (b) Data retention. The device was programmed in the ON and the OFF states by applying ±18.5 V respectively. Red and blue circles represent device current in the ON and the OFF states respectively. Filled and open circles correspond to short-circuit and constant read voltage protocols, respectively (see text) (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.).