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Stable organic static random access memory from a roll-to-roll compatible vacuum evaporation process

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ABSTRACT

An organic Static Random Access Memory (SRAM) based on p-type, six-transistor cells is demonstrated. The bottom-gate top-contact thin film transistors composing the memory were fabricated on flexible polyethylene naphthalate substrates. All metallization layers and the p-type semiconductor dinaphtho [2,3-b:2',3'-f] thieno[3,2-b]thiophene were deposited by thermal evaporation. The gate dielectric was deposited in a vacuum roll-to-roll environment at a web speed of 25 m/min by flash-evaporation and subsequent plasma polymerisation of tripropyleneglycol diacrylate (TPGDA). Buffering the TPGDA with a polystyrene layer yields hysteresis-free transistor characteristics with turn-on voltage close to zero. The static transfer characteristic of diode-connected load inverters were also hysteresis-free with maximum gain >2 and noise margin ~2.5 V. When incorporated into SRAM cells the time-constant for writing data into individual SRAM cells was less than 0.4 ms. Little change occurred in the magnitude of the stored voltages, when the SRAM was powered continuously from a −40 V rail for over 27 h testifying to the electrical stability of the threshold voltage of the individual transistors. Unencapsulated SRAM cells measured two months after fabrication showed no significant degradation after storage in a clear plastic container in normal laboratory ambient.

1. Introduction

The potential of organic/plastic electronics for fabricating large-area electronics (LAE) [1] on flexible substrates with different form factors, has created major new directions for electronic product design and applications. The key driver is the ability of organic materials to form robust films on thin, flexible substrates using low temperature production processes. Significant progress is now being made in fabricating circuits ranging from multistage ring oscillators (see for example [2–5] and references therein) and logic gates [6,7] through to 8-bit microprocessors [8], 8-bit transponders [9] and programmable logic arrays [10].

The ability to store data, either temporarily or semi-permanently, is an important requirement for many electronic circuit applications. Not surprisingly, then, many different types of organic memory devices have also been reported e.g. switchable resistive memory [11,12], floating gate memory devices [13] and memory transistors [14]. Also reported are organic versions of dynamic [15] and static [16–19] random access memory i.e. DRAM and SRAM respectively.

SRAM is an essential component of silicon-based electronics. For example, it is used in cache memories, microprocessors, systems-on-chip and applications for which speed is more important than capacity. Although SRAM is a volatile memory, so long as it is connected to a voltage supply, the stored data is stable for long periods and, unlike DRAM, does not require regular refreshing. Hence the larger cell area, accommodating two cross-coupled inverters and two access transistors (6-T SRAM), is partially compensated by removing the 'refresh' circuit requirement. Furthermore, in organic LAE applications, integration density is significantly lower than for silicon circuits so that achieving good operational speed is of greater importance than smaller cell size.

An early report on organic SRAM was by Takamiya et al. [17]

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who used a 12 × 12 array of 5-T write-only pentacene-based SRAMs to overcome the slow actuator transition rate in a Braille sheet display. The same approach was used in a later publication [18] in which faster SRAMs were fabricated from low-voltage transistors based on the more stable semiconductor dinaphtho[2,3-b:2′,3'-f] thieno [3,2-b]thiophene (DNTT) [20] deposited onto a thin aluminium oxide dielectric capped with a self-assembled monolayer [21]. Only a few other reports on SRAMs have appeared, notably by Kumar et al. [19] on the design and performance analysis of 6-T organic and hybrid (organic/oxide) SRAMs and Guerin et al. [16] who fabricated a complementary 6-T SRAM using p-type polytriarylamine and an n-type acene-diimide.

To date most organic circuits have been produced using small-scale laboratory-based techniques involving electrodes defined by shadow mask or photolithography and with the organic semiconductor deposited by spin-coating or vacuum-evaporation. A wide range of dielectrics have been used including both organic and inorganic, with the former generally being deposited by spin-coating. Solution-based mass-printing technologies have been reported [22,23] for organic LAE production. The best circuit performances, though, have been achieved using batch-processing approaches derived from silicon technology [5,24–26] and applied under clean room conditions. Such processes, however, require many deposition and patterning steps. For example, the basic transistor array reported by Sou et al. [10] required 10 process steps with additional steps then necessary for the e-display and ink-jet printed interconnects for programming the logic array.

It has been suggested that a vacuum roll-to-roll (R2R) process, in which all layers are vacuum-evaporated [27], could provide the route to fewer production steps and better circuit performance than achieved to date using mass-printing methods. Clear benefits of vacuum-evaporation include solvent-free production, high deposition rates and high yield. Furthermore, deposition and patterning methods compatible with R2R production are already available for each layer [27] and allow significant reduction in the number of process steps. In the following, we show that R2R-compatible, vacuum–evaporation processes can be used to produce stable organic SRAM arrays with good response times.

2. Experimental

Single 6-T SRAM cells and 4 × 4 SRAM arrays were fabricated on pre-cleaned 125 μm thick polyethylenenaphthalate (PEN) film (Dupont-Teijin Ltd). The circuits (Fig. 1) were based on p-type, bottom-gate top-contact thin film transistors (TFTs) fabricated using our previously described methods [3,6,28]. After the evaporation of aluminium gate electrodes and associated tracks, the 5 cm × 5 cm substrates were attached to the cooled drum of a webcoater (Aerre Machines) which rotated at a linear speed of 25 m/min. Tripropyleneglycol diacrylate (TPGDA) was then flash evaporated under vacuum onto the substrates and cross-linked *in situ* in a plasma discharge to form a robust dielectric layer, typically ~300 nm thick. To minimise the surface polarity of the TPGDA [29], a polystyrene (M_W = 350,000) film was spin-coated at 1000 rpm in a nitrogen glove box from a 3% wt:wt solution in toluene and annealed at 100 °C in air for 10 min yielding a capacitance C_i = 4.38 nF/cm^2 for the two-layer TPGDA-PS dielectric.

A 70 nm thick film of the air stable, high-mobility p-type organic small-molecule dinaphtho[2,3-b:2',3'-f] thieno[3,2-b]thiophene (DNTT) was evaporated onto the polystyrene followed by evaporation of the gold source-drain electrodes and associated tracks. Prior to this final step, vias through the polystyrene were created, in this case by mechanical scribing although an oxygen plasma etch has now been developed for future circuits. All layers apart from polystyrene were patterned by evaporation through shadow masks (Laser Micromachining Ltd) in order to minimise parasitic effects. Evaporation of metal and semiconductor layers was undertaken in a Minispectros vacuum evaporator (Kurt Lesker Ltd) integrated into a nitrogen glovebox. Polystyrene and TPGDA monomer were obtained from Sigma Aldrich. DNTT was synthesised using the method of Yamamoto and Takimiya [29] and purified by recrystallisation.

Single 6-T SRAM cells (Fig. 1(b)) as well as 4 × 4 arrays of cells (Fig. 2) were fabricated in this study. Each cell consisted of two cross-coupled inverters and two access TFTs to input and read stored data. The inverters were composed of a driver TFT and a diode-connected (enhancement) load TFT, the latter being possible owing to the negative threshold voltage of DNTT transistors produced using our method. In the single SRAM cell design, the load TFTs had a channel width, *W*, to channel length, *L*, ratio (*W/L*) of 625 μm/100 μm. For the access and driver TFTs, W/L = 2500 μm/50 μm. In the SRAM arrays, the corresponding values were 500 μm/50 μm and 4000 μm/50 μm respectively.

With the voltage supply, V_{DD} set to −40 V, data was stored in the cells by applying −40 V pulses to the word line (WL) to turn on the access TFTs and simultaneously applying pulses to the bit line (BL). The state of BL when WL turns off determines whether the stored data corresponds to logic 0 or logic 1. The stored data would normally be read by once again activating WL to turn on the access TFTs and reading the voltages on (or voltage difference between) BL and $\overline{BL}$. In this study, and in order to observe the state of the memory throughout the write/read process, the memory was also read directly at the inverters using probes to make contacts at the positions marked V_{OUT} and $\overline{V_{OUT}}$ in Fig. 1(b).

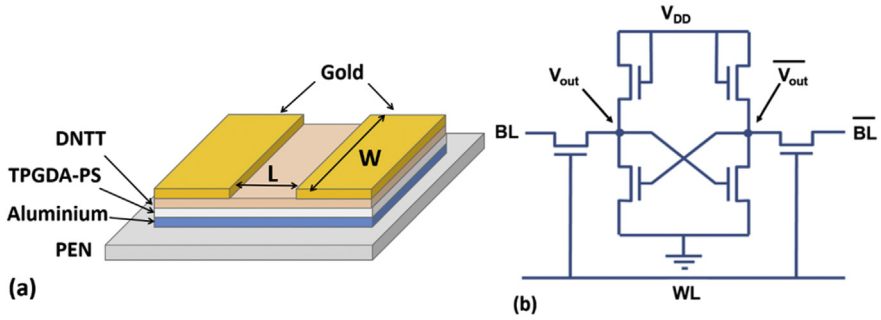

Fig. 1. (a) Structure of the vacuum-evaporated bottom-gate top-contact transistors used for fabricating the SRAM arrays. (b) Circuit diagram of a single SRAM cell. Data is written into and read from the cell via BL and $\overline{BL}$. During this investigation, the state of the SRAM was also monitored directly at the inverters connected to BL or $\overline{BL}$.