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Zirconium oxide dielectric layer grown by a surface sol–gel method for low-voltage, hysteresis-free, and high-mobility polymer field effect transistors

Byung Tack Lim [a], Jangwhan Cho [a], Kwang Hee Cheon [a], Kyu Min Sim [a], Kwonwoo Shin [b, **], Dae Sung Chung [a, *]

[a] School of Chemical Engineering and Material Science, Chung-Ang University, Seoul 156–756, Korea
[b] Energy Nano Materials Research Center, Korea Electronics Technology Institute (KETI), Seongnam 463-816, South Korea

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ABSTRACT

A simple, facile surface sol–gel method is introduced for the fabrication of zirconium oxide films for use as a dielectric layer of a solution-processed polymer field effect transistor (PFET). High dielectric strength is demonstrated for a zirconium oxide layer under room-temperature fabrication conditions using a surface sol–gel method without any post-treatments, which are typically needed in general sol–gel methods. X-ray photoemission spectroscopy showed that the fabricated zirconium oxide layer consists of inorganic ZrO_2 and organic alkoxide groups, which can explain its marginal dielectric constant (~9) and continuous film properties. In addition, by finishing the surface sol–gel synthesis at the stage of chemisorption, the hydrophobic nature of the final surface was retained, leading to a trap-free semiconductor/dielectric interface. As a result, the PFET made with a conventional polymeric semiconductor rendered nearly hysteresis-free and high mobility (0.3 cm^2/V) characteristics at low voltage (<2 V).

1. Introduction

Solution-processed metal oxides are attractive dielectric material candidates for high-performance polymer field effect transistors (PFETs) due to their high dielectric constant, and, thus, the possibility of low-voltage operation without compromising its high charge carrier mobility [1]. In the context of printed electronics, thin metal oxide layers that can be deposited via a solution-based, low-temperature process are of particular relevance [2]. Therefore, extensive research efforts have been undertaken to develop solution-processed metal oxides for gate dielectrics, low leakage current density, hydrophobic surface characteristics, large capacitance, and low-temperature processability [3]. Metal oxides of interest include titanium oxide [4], zirconium oxide [5], tantalum oxide [6], and hafnium oxide [7], all of which can be synthesized by a sol–gel method. For example, Park and coworkers demonstrated UV-based, room-temperature fabrication of ZrO_x layers for low-voltage operation of PFETs with a high hole mobility of 0.18 cm^2/V operating at <3 V [8]. Chung and coworkers used similar methods for the sol–gel synthesis of ZrO_x, but using a thermal annealing method, and demonstrated a high hole mobility of 3 cm^2/V operating at <1.5 V [9]. Although these achievements are impressive, one needs to note that the actual experimental procedures for these conventional sol-gel-based methods are not simple and can be divided into four steps: 1) sol–gel synthesis of metal oxides, 2) deposition of metal oxides, 3) curing the deposited metal oxide layer either by heat or UV, and 4) surface treatment of the metal oxide with a hydrophobic self-assembled monolayer [10–12]. Therefore, it would be useful to this the field if a more facile methodology for fabricating such metal oxide layers was developed while maintaining all other superior electrical and physical properties as dielectric layer.

The surface sol–gel method can be an efficient alternative method in which the chemisorption of a metal alkoxide and its hydrolysis are simply repeated to achieve the target thickness. Ichinose and coworkers reported on the surface sol–gel process of various metal oxide films with molecular precision. Several attempts have been made to strengthen the physical and electrical properties of films grown by the surface sol–gel method [13]. For example, Lu and coworkers introduced surface sol–gel processes

* Corresponding author.
** Corresponding author.
E-mail addresses: kwshin@keti.re.kr (K. Shin), dchung@cau.ac.kr (D.S. Chung).

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for the fabrication of thin (<5 nm) titanium oxide layers and then demonstrated low-voltage, high-mobility (~0.3 cm^2/V) FETs using pentacene as a semiconductor [14]. However, to the best of our knowledge, there has been no report on the fabrication of organic/polymeric FETs with ZrO_x grown by a surface sol–gel method. Over recent years, however, considering the superior electrical and physical properties of the surface sol–gel method, many efforts have been made to develop a low-temperature-processable ZrO_x layer so that it is compatible with plastic substrates. Here, we show that the surface sol–gel method is a good strategy for the fabrication of high-performance ZrO_x dielectric layers, even without post-treatments such as thermal or UV curing. By adapting the previously reported surface sol–gel method with molecular precision, we successfully deposited thin (~20 nm) ZrO_x layers with an ordinary dielectric constant of ~9, as well as high dielectric strength (break down voltage ~4 V). Of particular note, we completed the surface sol–gel synthesis during the chemisorption of alkoxide before hydrolysis so that the surface would possess hydrophobic characteristics even without any further surface treatment. By combining with a conventional polymeric semiconductor, poly(2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT), we demonstrated the fabrication of hysteresis-free, low-voltage (2 V), and high-mobility (0.3 cm^2/V) PFETs.

2. Experimental section

2.1. Surface sol–gel method

ZrO_x thin films were prepared by the surface sol–gel method as described earlier [13]. The piranha solution-treated bare Si wafer was used as a substrate. After plasma treatment, the Si wafer was dipped into zirconium propoxide ($Zr(O_nPr)_4$) solution (diluted in 1-propanol/toluene 1:1(v:v) solution, 100 mM) for 3 min. Then, to remove excess physisorbed alkoxide, the substrate was rinsed with 1-propanol for 1 min. For hydrolysis, the substrate was dipped into DI water for 1 min, and then dried with N_2 gas. This process was repeated 10 times to fabricate the target ZrO_x thin film (~20 nm).

2.2. Device fabrication

A Si wafer with a 100-nm-thick SiO_2 dielectric layer on heavily n-doped silicon was used for a reference sample. Poly(2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT, Aldrich) was used without further purification of the active layer material. The semiconducting polymer solution (trichlorobenzene, 0.4 wt%) was spin-coated at 3000 rpm to form films with a nominal thickness of ~50 nm, as confirmed by the surface profiler (Dektak 150, Veeco). To complete the PFET structure, thermally evaporated gold (80 nm) was deposited onto the prepared film as the source and drain electrodes. The channel length (150 μm) and width (1500 μm) were defined by a shadow mask.

2.3. Characterization of PFETs

Electrical characteristics of devices were measured in a N_2-filled glove box using HP4156A Semiconductor Parameter Analyzer. The capacitance was measured by Keysight E4981A at 1 KHz. The nominal thickness and morphology of the thin films were confirmed by a noncontact mode atomic force microscope (Park systems, NX20). The composition of ZrO_x thin films was confirmed

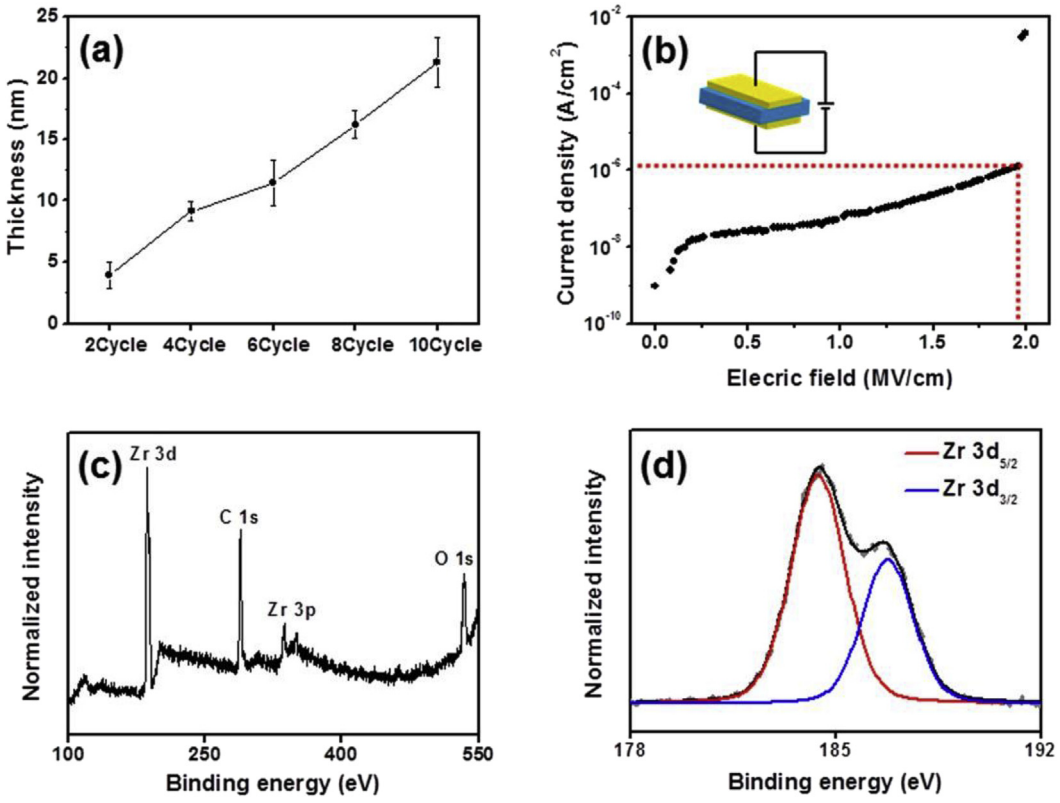

Fig. 1. (a) ZrO_x thin film thickness growth profile as a function of sequential LBL deposition process cycle count; (b) leakage-current density as a function of electric field for ZrO_x film (~20 nm) (red dotted line corresponds to break-down electric field) inset: schematic of MIM structure to measure leakage current; (c) XPS spectra of ZrO_x thin film and (d) high-resolution Zr 3d spectra (gray dotted line corresponds to raw data and red/blue line corresponds to fitting curves). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)