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Carrier transport and memory mechanisms of multilevel resistive memory devices with an intermediate state based on double-stacked organic/inorganic nanocomposites

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ABSTRACT

Multilevel resistive memory devices with an intermediate state were fabricated utilizing a poly(-methylmethacrylate) (PMMA) layer sandwiched between double-stacked PMMA layers containing CdSe/ZnS core–shell quantum dots (QDs). The current–voltage (I–V) curves on a Al/[PMMA:CdSe/ZnS QD]/PMMA/[PMMA:CdSe/ZnS QD]/indium-tin-oxide/glass device at low applied voltages showed current bistabilities with three states, indicative of multilevel characteristics. A reliable intermediate state was realized under positive and negative applied voltages. The carrier transport and the memory mechanisms of the devices were described on the basis of the I–V curves and energy band diagrams, respectively. The write-read-erase-read-erase-read sequence of the devices showed rewritable, nonvolatile, multilevel, and memory behaviors. The currents as functions of the retention time showed that three current states were maintained for retention times larger than 1×10^4 s, indicative of the good stability of the devices.

1. Introduction

The electrical characteristics of resistive nonvolatile memory devices based on organic materials have been extensively investigated for potential applications in wearable devices due to their simple fabrication, low cost, low-power consumption storage, and large mechanical flexibility [1–4]. However, organic resistive memory devices have inherent problems of low-density storage capability [5], slow switching speed [6,7], and inferior performance in comparison with inorganic memory devices [8]. The device performance of organic resistive memory devices has been significantly enhanced by utilizing hybrid organic structures [9,10], organic/inorganic composites [11,12], or multi-stacked layers [13–15]. In particular, multilevel nonvolatile memory devices are currently considered to be excellent devices for potential application to multi-value logic for high-speed computing and to ultra-high-density storage in portable devices.

Multilevel resistance tunability offers a unique opportunity to store more than 2 bits in a single cell, thereby achieving high-density memory with minimal downscaling. Therefore, research addressing the possibility of achieving multilevel resistive memory devices has attracted much attention. In addition, poly(-methylmethacrylate) (PMMA), due to its excellent chemical, physical, biological, and mechanical properties, has drawn considerable interest because of a desire to develop materials for applications in polymer-based memory devices [16]. Recently, CdSe/ZnS core–shell quantum dots (QDs) and graphene QDs have become particularly attractive due to their promising applications in high-efficiency electronic and optoelectronic devices [17,18]. However, resistive memory devices based on graphene QDs might not be a good choice due to their limited I–V curve ratios as reported in the literature [19]. The utilization of CdSe/ZnS core–shell QDs in resistive memory devices has been realized to stabilize memory performance, to decrease turn on voltage, and to reduce energy consumption. Furthermore, the on/off ratios of the I–V curves for resistive memory devices based on CdSe/ZnS core–shell QDs are larger than those for resistive memory devices based on graphene QDs [3]. Some investigations concerning the electrical characteristics of resistive nonvolatile memory devices containing core–-shell QDs embedded in a polymer layer or tristable resistive memory devices containing a double graphene charge trapping

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layer have been conducted [15,20,21]. However, very few studies of the carrier transport and memory mechanisms of multilevel nonvolatile memory devices based on double-stacked PMMA layers containing CdSe/ZnS core–shell QDs using a simple solution process have been performed. Furthermore, a stable intermediate state plays an important role for a multilevel memory device. In particular, the existence of intermediate states under positive and negative applied voltage might enhance memory performance.

This paper reports data for the carrier transport and memory mechanisms of multilevel resistive memory devices with an intermediate state based on double-stacked organic/inorganic nanocomposites. Scanning electron microscopy (SEM) measurements were conducted to demonstrate the formation of CdSe/ZnS QDs embedded in PMMA layers. Current–voltage (I–V) and switching measurements were performed to investigate the current bistability and the multilevel memory performance of the devices. The carrier transport and memory mechanisms of the Al/[PMMA:CdSe/ZnS QD]/PMMA/[PMMA:CdSe/ZnS QD]/indium-tin-oxide (ITO)/glass devices are described by using an energy-band diagram and I–V results. The retention characteristics of the multilevel current states for the devices were measured to investigate the stability of each multilevel current state.

2. Experimental details

PMMA:CdSe/ZnS QD nanocomposites were prepared by mixing a solution of CdSe/ZnS QDs (QD solution Nanodot-HE-100-630) in toluene and PMMA (CAS: 182265-25g) at a weight ratio of 49:1. Ultrasonic agitation was used to mix the solution for 4 h at room temperature. To prepare a PMMA solution, 60 mg of PMMA (CAS: 182265-25g) was added to 1.94 g of chlorobenzene (CAS: 184513-1L) followed by sonication for 4 h. This was done because we concluded that the PMMA layer should have a different solvent to avoid re-dissolution during the next spin-coating process. The ITO substrates were ultrasonically cleaned by using acetone and methanol and were then thoroughly rinsed in deionized water, each for 20 min. Next, the chemically-cleaned substrates were dried by using N_2 gas with a purity of 99.9999% in order to avoid any interaction with air. Fabrication of the memory device was begun with spin coating of a PMMA:CdSe/ZnS QD nanocomposite layer on top of the cleaned ITO substrate; after a wetting time of 10 s, spin coating was performed at 300 rpm for 10 s and then at 3000 rpm for 40 s to deposit the nanocomposite layer. This process was repeated for the second nanocomposite layer after the PMMA layer had been spin coated by using a PMMA solution on the first nanocomposite layer at 300 rpm for 10 s and then at 6000 rpm for 60 s. After each spin coating, each film was baked at 100 °C for 20 min to remove the existing solvents. Finally, the top Al electrodes with a diameter of 0.5 mm were deposited onto active films by using thermal evaporation. A schematic diagram of the structure for the Al/[PMMA:CdSe/ZnS QD]/PMMA/[PMMA:CdSe/ZnS QD]/ITO/glass devices used in this study is shown in Fig. 1(a). All electrical measurements were performed by using a Keithley 2400 unit at room temperature (300 K) in atmosphere.

3. Results and discussion

Fig. 1(b) shows an SEM image of the CdSe/ZnS QDs blended with a PMMA matrix. The SEM image shows that the CdSe/ZnS QDs were uniformly distributed in the PMMA layer without much aggregation, as shown in Fig. 1(b). The I–V characteristics of the fabricated device are shown in Fig. 2. The top Al electrodes were grounded, and the bias voltage was applied to the bottom ITO electrode. In the other way, it is believed that the charge injection is possibly easier from the Al electrode in comparison with the ITO electrode due to

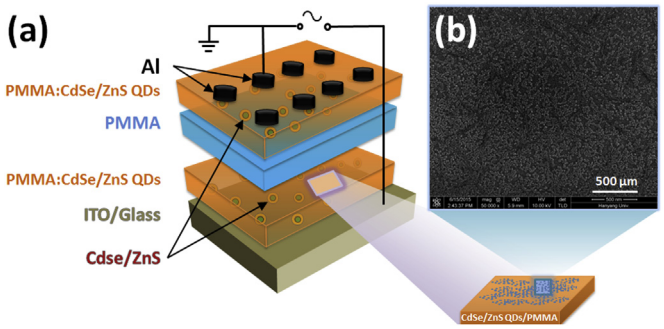

Fig. 1. (a) Schematic diagram of the Al/[PMMA:CdSe/ZnS QD]/PMMA/[PMMA:CdSe/ZnS QD]/indium-tin-oxide/glass device and (b) the scanning electron microscopy image of a single layer of CdSe/ZnS QDs embedded in a PMMA layer.

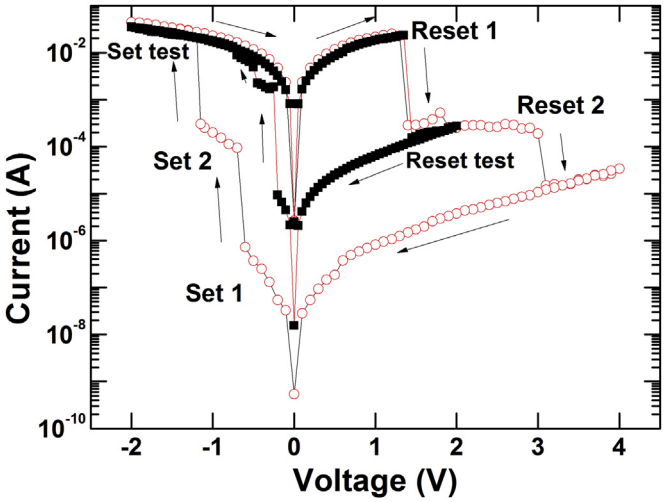

Fig. 2. Current–voltage curves of the Al/[PMMA:CdSe/ZnS QD]/PMMA/[PMMA:CdSe/ZnS QD]/indium-tin-oxide/glass device.

the lower work function of the Al [22]. The applied voltage across the device was swept from −2 to 4 to −2 V in all cases, as shown in Fig. 2. Devices clearly showed multilevel bistabilities at negative and positive voltages. At a writing voltage of about −0.7 V, the current abruptly increased, indicating a change from a low-conductivity (OFF) current state to an intermediate state; this change is denoted as Set 1 in Fig. 2. A decrease in the bias voltage to −1.2 V led to a second abrupt increase in the current, indicating a change from the intermediate current state to a high-conductivity (ON) current state. This change is denoted as Set 2 in Fig. 2. The current level of the device was maintained in a high-conductivity state during the voltage sweep from −2 to 0 V. When the applied voltage was swept from 0 to 4 V, at a bias voltage of 1.3 V, the current abruptly decreased, indicating a change from the high-conductivity state to the intermediate state; this change is denoted as Reset 1 in Fig. 2. A further increase in the bias voltage to above 3 V led to a second abrupt decrease in the current, indicating a change from the intermediate state to the low-conductivity state; this change is denoted as Reset 2 in Fig. 2. The I–V characteristics of the devices showed that there were two intermediate states with multilevel performances at applied voltages of −1.2 and 1.3 V. The I–V characteristics for the high-conductivity state and the intermediate state without the low-conductivity state when a Set test voltage of −2 V and a Reset test voltage of 2 V were applied to the device are shown as filled rectangles in Fig. 2. This result indicates