Organic Electronics 18 (2015) 107–112

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Letter

The effect of external electric field on the performance of perovskite solar cells

Xiaodong Li [a,c], Xueyan Wang [a,c], Wenjun Zhang [a], Yulei Wu [a], Feng Gao [b,*], Junfeng Fang [a,*]

[a] Ningbo Institute of Materials Technology and Engineering, Chinese Academy of Sciences, Ningbo 315201, China
[b] Department of Physics, Biology and Chemistry (IFM), Linköping University, Linköping SE-581 83, Sweden
[c] University of Chinese Academy of Sciences, Beijing 100049, China

ARTICLE INFO

Article history:
Received 12 December 2014
Received in revised form 7 January 2015
Accepted 18 January 2015
Available online 24 January 2015

Keywords:
Perovskite solar cells
External bias
Ion motion
Electric double layers

ABSTRACT

Planar heterojunction perovskite solar cells were fabricated through a low temperature approach. We find that the device performance significantly depends on the external bias before and during measurements. By appropriate optimization of the bias conditions, we could achieve an 8-fold increase in the power conversion efficiency. The significant improvement in device performance might be caused by the ion motion in the perovskite under the external electric field.

1. Introduction

The perovskite based materials ($CH_3NH_3PbX_3$, X = halogen) have attracted much interest for their promising application in solar cells as the light-absorbing component [1–3]. Initially, the perovskite solar cells employed an architecture similar to dye-sensitized solar cells (DSSCs) and a power conversion efficiency (PCE) of 3–4% was obtained [4]. Recently, with the optimization of device structure and materials design, substantial progress has been made [5–8], leading to the PCE exceeding 15% [7]. For this type of solar cells, the mesoporous metal oxides provide a scaffold on which the perovskite materials are grown. In addition, the scaffold also facilitates the electron transport from perovskite light-absorber to the electrodes [6,7]. Despite the high PCE, the mesoporous metal oxides usually require high temperature (~500 °C) to sinter, which is not compatible with flexible substrates.

Recently, Snaith and co-workers demonstrated that the planar heterojunction perovskite solar cells without mesoporous scaffold could also show a high PCE of 15.4% by a vapour deposition approach [9]. And the PCE up to 11.4% was also obtained through solution fabrication [10]. Compared with the previous DSSC structure with mesoporous scaffold, the planar heterojunction perovskite solar cells could be fabricated with much simpler process. However, for most state-of-the-art planar heterojunction perovskite solar cells, the perovskite light-absorber was deposited on a compact TiO_2 layer, which also required high temperature to sinter or crystallize [9–12]. Essentially, these planar heterojunction perovskite solar cells did not completely avoid the problems of high temperature mentioned above.

Soon afterwards, Jeng et al. demonstrated another type of planar heterojunction perovskite solar cells [13]. The perovskite materials were deposited on the ITO/PEDOT:PSS substrate, which made the structure similar to organic solar cells. Despite the relative moderate PCE of 3.9%, the easy fabrication and no need of high temperature treatment are attractive for decreasing the fabrication cost.

* Corresponding authors.
E-mail addresses: fenga@ifm.liu.se (F. Gao), fangjf@nimte.ac.cn (J. Fang).

http://dx.doi.org/10.1016/j.orgel.2015.01.024
1566-1199/

Afterwards, Sun et al. increased the PCE to 7.4% through two-step deposition of perovskite materials [14]. In addition, the groups of Snaith, Yang and Bolink also reported low temperature fabricated planar perovskite solar cells and PCEs approaching or over 10% were obtained [15–18]. In such a short time (less than 1 year), the PCE of planar heterojunction perovskite solar cells significantly increased from ~4% to over 10%, indicating promising future for planar perovskite solar cells.

In spite of significant improvement in device performance of perovskite solar cells, understanding of the operation mechanisms is still in progress [19–21]. For example, the mechanisms behind efficient charge generation, high open-circuit voltage, and anomalous hysteresis in the *J–V* curves are not clear yet. Here, we fabricated planar perovskite solar cells on the ITO/PEDOT:PSS substrates (Fig. 1). We found that the external bias plays a critical role on the device performance. By applying an external bias prior to the device measurement, the PCE could be significantly increased from ~1% to over 8%. In addition, the test conditions, e.g. the scan bias range, could also effectively affect device performance. We propose that that the ion motion in the perovskite might be responsible for the behavior observed.

2. Material and methods

2.1. Synthesis of CH_3NH_3I

CH_3NH_3I was synthesized through the reaction of 24 mL methylamine (33 wt.% in ethanol, Aldrich) and 10 mL hydroiodic acid (57 wt.% in water, Aladdin, China) in 100 mL ethanol at ice bath for 2 h with stirring. The precipitate was collected with a rotary evaporator at 50 °C to exclude the solvent. Then the produce was recrystallized in ethanol. The crystals were filtered and washed with diethyl ether three times. At last, the solid was dried at 60 °C in vacuum oven overnight.

2.2. Fabrication of perovskite solar cells

ITO glass was cleaned with ultrasonic treatment in deionized water, acetone and isopropanol for 15 min, respectively. Then the substrates were dried with N_2 flow and further cleaned with UV–ozone for 20 min. Next, PEDOT:PSS (Clevios 4083) was spin-coated on ITO substrates at 4000 rpm 60 s and heated at 140 °C 15 min in air. After that, the substrates were transferred to glovebox (filled with N_2). Perovskite precursor solution was prepared by dissolved CH_3NH_3I and $PbCl_2$ with molar ratio of 3:1 in DMF (40 wt.%) at 60 °C. Then the solution was deposited on ITO by spin-coating at 2000 rpm for 45 s. After spin-coating, the substrates were left in glovebox for 1 h, and then annealed at 100 °C for 1 h. At last, the substrates were transferred to vacuum chamber (10^{-6} mbar) and 20 nm fullerene (C60, Aldrich) and 100 nm Al was deposited as cathode. The device area was 4 mm^2.

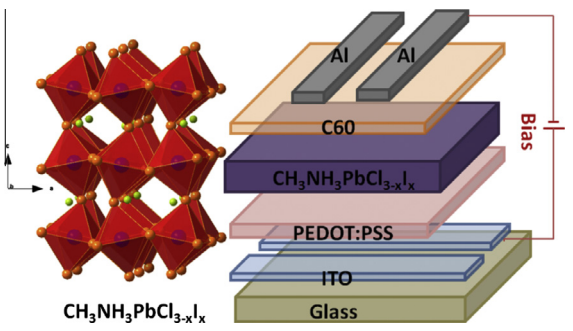

Fig. 1. The structure of the perovskite ($CH_3NH_3PbCl_{3-x}I_x$) and the device configuration used in our work.

2.3. Device characterization

The *J–V* measurements were carried out using Keithley 2440 sourcemeter controlled by a computer. All the solar cells were measured under simulated AM 1.5G spectrum (100 mW/cm^2) with an Oriel So13A solar simulator. Note that all the devices were measured from positive bias to negative bias.

3. Results and discussion

Fig. 2 shows the *J–V* curves with different scan bias range (the scans are from the positive bias to negative bias) for the same device. The fresh device shows poor performance (PCE of 0.13%) under −1 to 1 V scan range, mainly due to the inferior V_{oc} of 0.183 V, J_{sc} of 2.59 mA/cm^2, FF of 27.0%. When we measure the device with scan range of −1 to 2 V, the V_{oc} (0.445 V), J_{sc} (9.04 mA/cm^2), and FF (32.9%) all increase, leading to a moderate PCE of 1.32%. And when the scan range of −1 to 6 V is applied, a PCE of 4.29% is obtained with a V_{oc} of 0.708 V, J_{sc} of 15.34 mA/cm^2, and FF of 39.5%. However, when larger scan range of −1 to 8 V is applied, both the V_{oc} (0.695 V) and FF (37.0%) decrease, resulting in a decreased PCE of 4.04% despite slightly increased J_{sc} of 15.71 mA/cm^2. All the results above clearly indicate that the scan bias range plays a critical role on the device performance. The larger scan bias range leads to better performance (from 0.13% at −1 to 1 V to 4.29% at −1 to 6 V). But if the scan bias range is too large (e.g. −1 to 8 V), the large injection current density may destroy the device, thus resulting in decreased performance.

To further understand the effect of external bias on device performance, we directly apply a bias on the device before the measurement (the direction of bias is shown in Fig. 1). The external bias is applied on the devices under dark conditions. We first investigate the effect of the bias direction on device performance (Fig. S1) and find that positive bias could significantly improve device performance, while negative bias decreases the performance, which agrees with the enhanced performance under large positive scan bias range mentioned in Fig. 2. We then turn to the relation between the bias value and device performance, and the results are shown in Fig. 3. The fresh device under the scan bias range of −0.5 V to 1.5 V shows poor performance with PCE of 0.79%. When a constant positive bias of 1 V is applied on the same device for 30 s, the performance could be slightly increased and a PCE of 1.10% is