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Low power flexible organic thin film transistors with amorphous $Ba_{0.7}Sr_{0.3}TiO_3$ gate dielectric grown by pulsed laser deposition at low temperature

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ABSTRACT

We deposited amorphous $Ba_{0.7}Sr_{0.3}TiO_3$ (BST) on silicon and plastic substrate under 110 °C by pulsed laser deposition (PLD) and use it as the dielectric of the organic transistor. Depends on the thickness of BST layer, the highest mobility of the devices can achieve 1.24 $cm^2 V^{-1} s^{-1}$ and 1.01 $cm^2 V^{-1} s^{-1}$ on the silicon and polyethylene naphthalate (PEN) substrate, respectively. We also studied the upward and downward bending tests on the transistors and the dielectric thin films. We found that the BST dielectric pentacene transistor can maintain the mobility at 0.5 $cm^2 V^{-1} s^{-1}$ or higher while the bending radius is around 3 mm in both upward and downward bending. Our finding demonstrates the potential application of PLD growth high-k dielectric in the large area organic electronics devices.

Due to the flexibility, light weight and compatible with large area fabrication, organic electronics have received considerable attention in the past decades. Among different organic devices, organic thin film transistor (OTFT) have been considered as the key component in the plastic electronic circuits [1,2], and their applications cover active matrix display, radio frequency identification (RFID), memories or circuit processors [3–5]. In terms of device performance, although some OTFTs have shown comparable mobilities with amorphous silicon devices, it still need further reduction on the operating power of the devices especially for the battery-powered and portable devices, and a commonly adopted approach is by increasing the capacitance per unit area (C') of the dielectric insulators. As the C' is given by $C' = \varepsilon\varepsilon_0/t$ where ε_0 is the permittivity of vacuum, ε and t are the dielectric constant and thickness of the insulator material, respectively; the value of C' can be increased by either decreasing the thickness of the insulator layer or by employing an insulator with higher dielectric constant (high-k). The reduction of the thickness is challenging for low dielectric constant materials ($\varepsilon \leqslant 4$) such as PMMA or SiO_2 because it usually requires the dielectric layer to be extremely thin and the leakage current can be significant even if a small amount of defects exists. Self-assembly monolayers (SAMs) is an effective solution for reducing the dielectric thickness [6]. In the SAMs, the head group are specially designed for attaching onto particular gate dielectric insulator or gate electrodes by chemical bonding, while the terminating groups on the other hand control the growth morphology and the packing of the organic semiconductors (OSC). As the packing of the OSC affects the leakage current of the OTFTs, the terminating group hence also affects the leakage current. For example,

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the leakage current of pentacene transistor with acene group as the terminating group shows 100 times reduction while comparing with the aromatic group [7]. However, as the head and terminating groups of the SAMS may only work for particular gate electrodes, dielectric insulators or organic semiconductors, different SAMs are required for various transistors; furthermore, it is also difficult to apply SAMs in the OTFTS with the top gate electrode configurations. On the other hand, for the employment of high permittivity dielectric insulators, OTFT fabricated on high-k dielectric such as metal oxides have also shown their potentials on reducing the operating voltage. Pentacene OTFTs with aluminum oxide (Al_2O_3) grown by sol–gel method [8], and hafnium oxide (HfO_2) grown by atomic layer deposition [9] have shown low operating voltages at around 3 V, but the high processing and annealing temperature for solvent removal and crystallization of the dielectric may limit their applications on flexible substrates with low glass transition temperatures.

Similar to the sol–gel method with high annealing temperature (>700 °C) [10], high substrate temperature pulsed laser deposition (PLD) is usually applied for growing crystalline $Ba_{0.7}Sr_{0.3}TiO_3$ (BST) with high dielectric constant ($\varepsilon > 200$) and under low oxygen pressure environment [11]. Due to the ferroelectric properties of the crystalline BST films, they can be used as tunable capacitors [12], optical modulator [13] or microwave circuit components [14]. However, as the crystal grains and the boundaries hinder the growth of the organic semiconductors, it is difficult to apply crystalline BST as the OTFT dielectric insulators. To overcome the morphology effect induced by the crystalline BST, amorphous BST prepared by solution processing under lower annealing temperature (400 °C) have been employed as dielectric of OTFT on silicon substrate [15]. Although the roughness of the dielectric surface is significantly reduced in the amorphous BST and the field effect mobility (μ_{FE}) of the pentacene can achieve 0.16 $cm^2\ V^{-1}\ s^{-1}$ [15], the processing temperature is still too high for the plastic flexible substrates which usually have the glass transition temperatures at 200 °C or lower. To overcome this, Dimitrakopoulos et al., also demonstrates the fabrication of amorphous barium zirconate titanate (BZT) by using room temperature magnetron sputtering method on flexible polycarbonate substrate [16]. The device shows a higher mobility (μ_{FE} = 0.38 $cm^2\ V^{-1}\ s^{-1}$) but the saturation properties in the output curves is weaker than the solution processing device and it could be due to the fact that larger surface roughness in the magnetron sputtering films hence larger leakage current in the device.

In this study, we demonstrated a low temperature high-k dielectric processing technique which can be applied on plastic substrates. Low operating power OTFTs are fabricated on amorphous BST with a smooth surface (roughness <0.2 nm). The BST thin films are growth by PLD under low processing temperature (110 °C) and the capacitance per unit area of the thin films at low frequency can achieve ca. 300 nF cm^{-2}. The pentacene OTFTs have threshold voltage around 1 V, field effect mobility as high as 1.24 $cm^2\ V^{-1}\ s^{-1}$ (on silicon) and 1.01 $cm^2\ V^{-1}\ s^{-1}$ (on flexible substrate), operating voltage <3 V and on/off ratio >1×10^4 (both silicon and flexible substrates). Although the current BST are deposited on silicon and polyethylene naphthalate (PEN) substrates with an area just 6.55 cm^2 (1 in. × 1 in.), the PLD deposition method has been demonstrated for deposition of thin films with a much larger area before [17,18]. Moreover, the BST dielectric is compatible with both top and bottom gate contact configurations, as well as various fabrication techniques other than thermal evaporation such as solution processing and vapor jet deposition [19]. To the best of our knowledge, it is the first demonstration of amorphous BST thin film grown by PLD at low temperature for flexible OTFT applications. The stable performance of the OTFT under bending test shows its potential for flexible electronics.

The PLD deposition of the BST is performed under pressure of 2×10^{-3} Pa while the substrate holder keeps at 110 °C as shown in the schematic diagram of the PLD system in Fig. 1(a). Low pressure environment is used for preventing the oxidization of the hydrofluoric acid treated silicon substrates. The 248 nm KrF excimer laser with a repetition frequency of 10 Hz, pulse width of 10–50 ns and the corresponding energy per pulse 250 mJ is used as the source. The distance between the target and the substrate holder is maintained at 5 cm and the thickness of the BST thin film is controlled by the growth time. Fig. 1(b) shows the atomic force microscope (AFM) (Digital Instrument, NanoScope VIII) image of the BST thin film deposited on heavily doped n-type silicon. It can be noticed that the amorphous BST film forms a smooth surface (RMS roughness is less than 0.2 nm). The amorphous nature is confirmed by the XRD (Rigaku Smartlab 9KW) measurements of the BST thin film on silicon substrate (Fig. 1(c)), where only peaks from the Si can be detected on the BST/Si substrate; it agrees with the results observed by Dong and co-workers [20]. To further investigate the interface quality between the silicon substrate and the BST thin film, we applied high resolution transmission electronic microscope (TEM) (Philips Tecnai G220 S-TWIN) to study the cross sectional image of the interface between the BST and Si substrate. As shown in Fig. 1(d), the amorphous BST is grown on the silicon evenly without crystallization and the amorphous nature of the BST can be clearly deviated from the highly crystallized silicon substrate. The dielectric properties of the BST thin films are characterized by C'–f measurements under the metal–insulator–metal (MIM) structure, in which 600 μm diameter circular Ag top contacts are thermal evaporated onto the BST thin film on the n^+-Si substrate. As shown in Fig. 1(e), the areal capacitances of the thinnest (96 nm) and thickest (770 nm) BST films used in our experiment maintain at relative constant values in the high frequency regime from 10 kHz to 1 MHz. However, in the low frequency regime, the capacitance of the 96 nm film increases from 180 nF cm^{-2} at 1000 Hz to 261 nF cm^{-2} at 40 Hz. The increase of capacitance at lower frequency regime of the 770 nm BST film is more significant and the capacitance increases from 46 nF cm^{-2} at 1000 Hz to 114 nF cm^{-2} at 40 Hz. It is interesting to notice that the capacitance decrease of the films is not proportional to the film thickness which suggests varying combination in thicker films and dead layer effect may exist in the films [21]. The increase