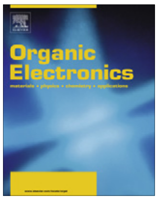
Organic Electronics 12 (2011) 1370–1375

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel



Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with improved performance and stability

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ARTICLE INFO

Article history:
Received 9 February 2011
Received in revised form 27 April 2011
Accepted 28 April 2011
Available online 19 May 2011

Keywords:
Organic thin-film transistors
Air stability
Bias–stress stability

ABSTRACT

Organic thin-film transistors based on the vacuum-deposited small-molecule conjugated semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) have been fabricated and characterized. The transistors have field-effect mobilities as large as 2 cm^2/V s and an on/off ratio of 10^8. Owing to the large ionization potential of DNTT, the TFTs show excellent stability for periods of several months of storage in ambient air. Unipolar ring oscillators based on DNTT TFTs with a channel length of 10 μm oscillate with a signal propagation delay as short as 7 μsec per stage at a supply voltage of 5 V. We also show that DNTT TFTs with usefully small channel width/length ratio are able to drive blue organic LEDs to a brightness well above that required for active-matrix displays.

Organic thin-film transistors (TFTs) are of interest for rollable or foldable active-matrix displays [1–4], conformable sensor or actuator arrays [5–8], and flexible identification tags [9,10]. One of the challenges in the development of organic TFTs is to find a conjugated semiconductor that provides both a large field-effect mobility and a good stability during operation in ambient air. For many years, the small-molecule hydrocarbon pentacene has enjoyed immense popularity, because pentacene TFTs can be operated in air and initially provide relatively large mobilities, usually around 1 cm^2/V s or above [1–10]. The main problem with pentacene is that the molecules easily oxidize in air [11], so that the field-effect mobility decreases over time when the devices are exposed to air. The air-induced mobility degradation can be avoided by encapsulation [12–15], but from the standpoint of manageable process complexity, a conjugated semiconductor with a strong intrinsic resistance against oxidation is very desirable. With this in mind, a fused heteroarene, dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) has recently been synthesized that is characterized by a larger ionization potential (and hence better air stability) than pentacene, and by a crystal structure and thin-film morphology that promotes high-mobility charge transport, similar to pentacene [16–19].

Here we report on the performance and stability of inverted staggered (bottom-gate, top-contact) DNTT TFTs that utilize a high-capacitance gate dielectric which allows the transistors to operate with voltages of about 3 V [20–23]. The initial field-effect mobility extracted from the transfer characteristics of the TFTs is 2.1 cm^2/V s when the channel length is sufficiently long (50 μm) so that the influence of the contact resistance on the device resistance is negligible, and 1.2 cm^2/V s for shorter channel length (10 μm). These mobilities are slightly larger compared

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doi:10.1016/j.orgel.2011.04.018

with the mobilities previously reported for low-voltage DNTT TFTs [23]. Compared with the previous report [23] the thickness of the DNTT layer has been reduced from 30 to 25 nm, which is expected to reduce the parasitic potential drop associated with the vertical current path between the source/drain contacts (located on top of the semiconductor) and the carrier channel (located at the bottom of the semiconductor) and hence is expected to increase the transconductance and effective mobility of the TFTs [24].

The TFTs and circuits were fabricated on glass (Corning Eagle 2000) or flexible polyethylene naphthalate (Teonex® Q65 PEN; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, UK). Aluminum with a thickness of 20 nm was evaporated directly onto the substrate through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) to define the gate electrodes. The aluminum was briefly exposed to an oxygen plasma to create a 3.6 nm thick AlO_x film, followed by immersion of the substrate in a 2-propanol solution of *n*-tetradecylphosphonic acid to form a 1.7 nm thick self-assembled monolayer (SAM) on the surface of the oxidized gates. This results in an AlO_x/SAM gate dielectric with a thickness of 5.3 nm and a capacitance of 800 nF/cm^2 [25–27]. A 25 nm thick DNTT layer was vacuum-deposited through a shadow mask, followed by the deposition of 30 nm thick gold through another shadow mask to define the source/drain contacts. The channel length is between 10 and 50 µm and the channel width is 100 µm or 200 µm. The maximum process temperature is 60 °C (the substrate temperature during the DNTT deposition). Fig. 1. shows the chemical structure of the semiconductor DNTT, a schematic cross-section of the TFTs, and photographs of a TFT with a channel length of 10 µm. All electrical measurements, including the shelf-life and bias–stress measurements, were performed in ambient air at room temperature.

The static performance of the flexible DNTT TFTs measured shortly after fabrication is summarized in Fig. 2. The TFTs have an on/off ratio of 10^8 and a subthreshold swing of 100 mV/decade. For the shortest channel length ($L = 10$ µm), the transconductance (normalized to the channel width) reaches 0.12 S/m. This is a factor of three larger than the transconductance of pentacene TFTs based on the same fabrication process and the same channel length fabricated on glass substrates [20] and similar to the transconductance of photolithographically patterned bottom-contact pentacene TFTs with a channel length of 5 µm on flexible polymeric substrates recently reported by the IMEC group [10]. The field-effect mobility extracted from the transfer characteristics of our DNTT TFTs in the saturation regime ranges from 1.2 cm^2/V s ($L = 10$ µm) to 2.1 cm^2/V s ($L = 50$ µm). The observation that the mobility extracted from the transfer characteristics decreases with decreasing channel length indicates that the relative contribution of the contact resistance to the total device resistance increases with decreasing channel length. This effect has been analyzed in detail for pentacene TFTs [28] and is expected to be even more pronounced for DNTT TFTs, since the larger ionization potential of DNTT (5.4 eV) compared with pentacene (5.0 eV) [18] is expected to produce a larger energy barrier at the interface between the semiconductor and the Au source and drain contacts (Fermi energy about 5 eV), and hence a larger contact resistance.

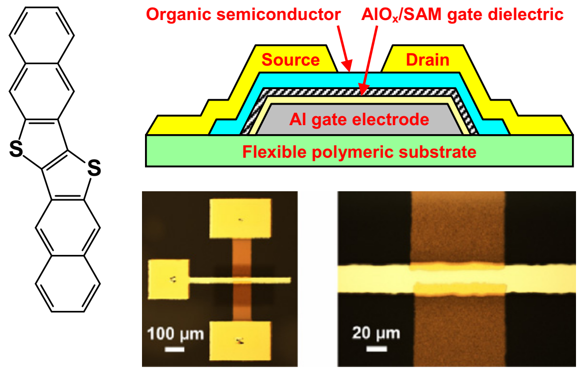

Fig. 1. Chemical structure of the conjugated organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT), schematic TFT cross-section, and photographs of a DNTT TFT with a channel length of 10 µm and a channel width of 100 µm patterned using polyimide shadow masks.

Fig. 3a. shows how the saturation mobility of a flexible DNTT TFT with a channel length of 50 µm evolves over time when the substrate is kept in ambient air with a humidity of 40–70% under weak yellow light (laboratory conditions). The mobility decreases from initially 2.1 to 2.0 cm^2/V s after three months and then to 1.5 cm^2/V s after a total of eight months in air. For comparison, Fig. 3a. also shows that the DNTT TFTs have substantially better air stability than pentacene TFTs fabricated with the same technology (i.e., same type of substrate, same gate dielectric, same contacts).

Although the air stability of the DNTT transistors is better than that of the pentacene devices, there is a slight drop in the mobility of the DNTT TFTs, from initially 2.1 to 1.5 cm^2/V s after eight months in air. The mechanism for this slow degradation is unknown. Although oxidation of the DNTT molecules cannot be completely ruled out, it is unlikely given the molecular structure of DNTT. An alternative explanation for the observed mobility degradation is that air-borne molecules (e.g., H_2O, O_2, O_3) penetrate into the grain boundaries of the polycrystalline DNTT film and then interact with the mobile charge carriers or with the DNTT molecules at or near the grain boundaries in a way that is detrimental for the field-effect mobility [29,30].

In addition to the shelf-life stability we have also investigated the bias–stress stability. Fig. 3b illustrates the time-dependent decrease in drain current and the associated shift in threshold voltage of DNTT TFTs fabricated on a glass substrate during prolonged gate–bias stress. As in the case of TFTs based on hydrogenated amorphous silicon [31,32] and pentacene [33] the drain current decays faster when the applied gate–source voltage is larger. The reason is that a larger gate–source voltage results in a larger carrier density in the channel and hence in a larger trapping rate. The carrier density accumulated in the transistor channel at a certain gate–source voltage can be estimated as follows:

$$n = \frac{1}{q} C_{\mathrm{diel}} |V_{\mathrm{GS}} - V_{\mathrm{th}}| \tag{1}$$