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Vertically stacked hybrid organic–inorganic complementary inverters with low operating voltage on flexible substrates

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ABSTRACT

Hybrid organic–inorganic complementary inverters were demonstrated on a flexible polyethersulfone (PES) substrate with vertically stacked *p*-channel pentacene and *n*-channel amorphous indium gallium zinc oxide thin-film transistors (TFT). Al_2O_3 layers grown by atomic layer deposition were used as top- and bottom-gate dielectric layers. Common-gate top-contact *p*- and bottom-contact *n*-channel TFTs showed saturation mobility values of 0.3 ± 0.02 and 5.3 ± 0.2 cm^2/Vs and low threshold voltage values. Complementary inverters yielded high gain values of 61 V/V with high and balanced noise margins at a low supply voltage of 5 V. The independent control of the thickness of the gate dielectric layer used for each transistor in this proposed vertically stacked geometry, allows for the realization of high-density low-power complementary circuits with high gain and balanced noise margins.

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1. Introduction

Thin-film transistors recently have attracted considerable attention as an emerging technology for unique consumer markets that will allow the development of microelectronic circuits on flexible substrates, over very large-areas and potentially at a very low cost. Organic and oxide-based TFTs are two technologies that offer advantages over *n*-channel amorphous silicon TFTs technologies in that these materials are capable of larger mobilities, can be processed at lower temperatures [1–4] and if combined, they could lead to complementary electronic circuits. To date, most complementary inverters used two-dimensional (2D) geometries. Recently a vertically stacked organic TFT-based inverter was demonstrated using two *p*-channel transistors on a glass substrate [5]. This vertical inverter with two pentacene TFTs stacked on top of one another yielded a maximum gain of 13.4 V/V and a switching threshold voltage of −11 V with noise margin low and high values of 9.4 and 6.6 V, respectively, at a supply voltage of 20 V. However, practical electronic devices are expected to use *p*- and *n*-channel TFT-based complementary inverters to operate with low power consumption, high gain, high noise margins, and on flexible substrates.

Organic materials provide a natural framework for the development of complementary technologies, since *n*-channel or *p*-channel TFTs can readily be fabricated. However, they tend to be more susceptible to degradation in air and have lower mobilities than metal oxide semiconductors. On the other hand, transistors based on oxide semiconductors that can be processed at low temperatures with high mobility values operate mainly as *n*-channel transistors [3,6,7]. Hence, hybrid complementary structures comprising *p*-channel organic and *n*-channel metal oxide TFTs are particularly attractive to realize complementary circuit designs because they benefit from the intrinsic advantages of these two material systems.

Most hybrid TFT-based complementary inverters use horizontally distributed *n*- and *p*-channel semiconductor layers with a bottom-gate geometry [8–10] with a shared gate dielectric layer. Recently, we demonstrated organic–inorganic hybrid complementary inverters with high gain

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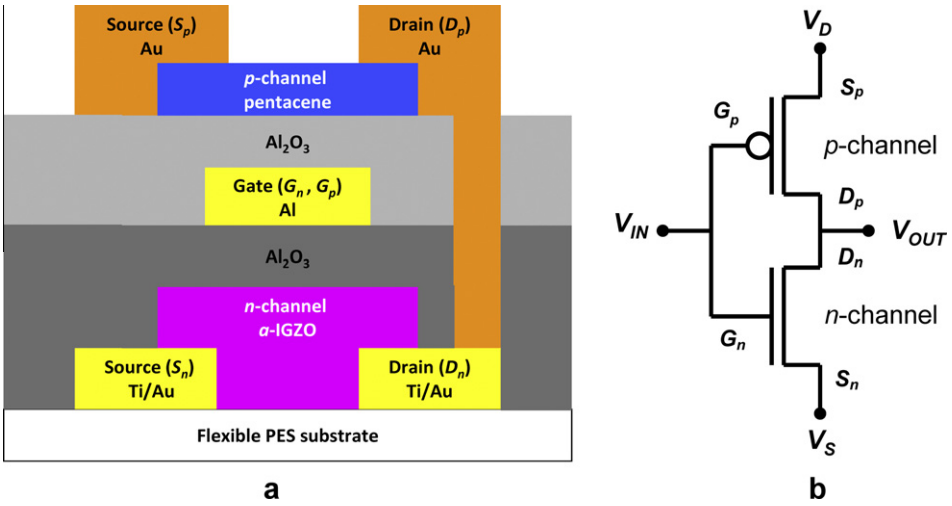

Fig. 1. (a) Schematics of the complementary inverter with vertically stacked pentacene and amorphous *a*-IGZO thin-film transistors on a flexible polyethersulfone substrate. (b) Complementary inverter circuit diagram.

values of 130 V/V and high and balanced noise margins employing *n*-channel *a*-IGZO and *p*-channel pentacene TFTs horizontally distributed on flexible substrates [10]. Here, we report on a novel flexible hybrid organic–inorganic vertically stacked complementary inverter geometry in which a *p*-channel pentacene TFT is stacked on top of an *a*-IGZO *n*-channel TFT. This geometry shown in Fig. 1 has the following advantages. The potential damage to the organic semiconductor layer associated with the deposition of gate dielectric materials and further fabrication steps of the *n*-channel TFT is avoided by employing a *p*-channel organic TFT on the top of a burried *n*-channel oxide TFT. Furthermore, the thickness of each of the gate dielectric layer used for the *n*- and *p*-channel TFTs can be controlled independently which is an important design parameter to achieve complementary circuits with high gain and balanced noise margins. In this study, a 100 nm-thick Al_2O_3 was used as top-gate dielectric for the *n*-channel oxide TFT and a 75 nm-thick Al_2O_3 was used as bottom-gate dielectric for the *p*-channel organic TFT. In both cases, atomic layer deposition was used to grow the Al_2O_3 layers. Balanced "*on*-currents" at the same operating voltages were obtained by independently controlling the size and width of the *n*- and *p*-channels, and by adjusting the thickness of the Al_2O_3 layers.

2. Device fabrication and electrical characterization

Hybrid organic–inorganic complementary inverters with vertically stacked TFTs were fabricated on a flexible polyethersulfone (PES) substrate. A bottom-gate top-contact *p*-channel TFT was fabricated on the top of a top-gate bottom-contact *n*-channel TFT by sharing the gate electrode, as shown in Fig 1(a). First, Ti/Au (6 nm/50 nm) electrodes were deposited using electron-beam (e-beam) at room temperature on a glass substrate through a shadow mask to define the source and drain electrodes for the top-gate *n*-channel TFT. A 30 nm-thick *a*-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:1 mol%) layer was then deposited by radio frequency (rf) sputtering without intentional substrate heating using a power of 125 W, a working pressure of 3 mTorr, and an O_2/Ar (2/98) atmosphere through a shadow mask. Then, a 100 nm-thick Al_2O_3 gate dielectric layer was deposited by atomic layer deposition (ALD) system (Savannah100, Cambridge Nanotech Inc.) on top of the *a*-IGZO to form a TFT with a top-gate geometry. The Al_2O_3 films were deposited at 110 °C using alternating exposures of tri-methyl-aluminum ($Al(CH_3)_3$) and H_2O vapor at a deposition rate of approximately 0.1 nm per cycle. Each deposition cycle (one monolayer) lasted 25 s, yielding a total deposition time of 7 h and 20 min for 1000 cycles [11]. Al_2O_3 layers deposited by ALD had a dielectric constant of nine, which yielded highly conformal and defect-free gate dielectrics with high capacitance densities [12,13]. A 50 nm-thick Al electrode was fabricated by thermal evaporation through a shadow mask to serve as a common gate electrode. Then, another 75 nm-thick Al_2O_3 was deposited by ALD on the top of the *n*-channel *a*-IGZO TFT to serve as the gate dielectric for the pentacene TFT. A 50 nm-thick layer of pentacene was deposited through a shadow mask using thermal evaporation at a substrate temperature of 25 °C and an initial pressure of 2×10^{-8} Torr. Prior to its thermal evaporation, pentacene was purified using gradient zone sublimation. Finally, Au (100 nm) source/drain electrodes were deposited through a shadow mask over the pentacene channel. Here, a small offset, of around 400 μm, was introduced along the channel width direction to allow independent access to the source and drain electrodes of the top and bottom TFTs. This offset is not necessary but was use to facilitate the individual characterization of both TFTs. The samples were then transferred into a nitrogen-filled glove box (O_2, H_2O <0.1 ppm) for electrical testing. Gold was used as source and drain electrodes because it provides a similar charge-injection energy barrier of 0.6 eV for the injection of holes into pentacene and electrons into *a*-IGZO [14,15]. In these complementary inverters with a vertical stacked