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Letter

Fast, simple ZnO/organic CMOS integrated circuits

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ABSTRACT

Hybrid organic–inorganic CMOS thin-film circuits are a simple, potentially low-cost, approach for large-area, low-power microelectronic applications. We have used atmospheric pressure processes to deposit inorganic ZnO and organic diF TES-ADT semiconductor layers and an Al_2O_3 gate dielectric. The organic semiconductor uses a contact-treatment-related microstructure that allows circuits to operate without directly patterning the organic layer. Using a simple 4-mask process with bifunctional Ti/Au contacts for both ZnO and organic transistors, 7-stage ring oscillators were fabricated and operated at >500 kHz corresponding to a propagation delay of <150 ns/stage at a supply bias of 35 V. These are the fastest organic–inorganic CMOS circuits reported to date.

1. Introduction

The demand for low-cost, high-mobility, thin-film transistor (TFTs) technologies has generated particular interest in low-temperature-process organic and metal oxide semiconductors. CMOS circuits are likely to be important for low-power and especially battery-powered applications and also because CMOS allows simplified and more robust circuit design. In particular, low-cost, low-temperature device fabrication processes often result in devices with a distribution of characteristics. For unipolar circuits this typically results in digital circuits with varying response to input signals and varying output voltages. While this can be accommodated to some extent by appropriate circuit design, the result is often slower, less reliable, and lower yield circuits. Because CMOS digital circuits use complementary switches, they typically provide output logic levels at or close to the power supply rails. This allows many CMOS digital circuits to tolerate large deviations from ideal device behavior and substantial variation in device-to-device characteristics.

ZnO is currently one of the most promising n-type semiconductors for thin-film applications because it allows high-quality thin films and high-mobility TFTs (>10 cm^2/V s) using low-temperature deposition processes. How-

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ever, while n-channel ZnO TFTs have been widely reported (for example, [1,2]), there are no reports of stable, high-mobility, p-channel devices. In contrast, p-channel organic TFTs typically have higher mobility and better stability than n-channel organic devices. While the stability and field-effect mobility of most organic TFTs are poor compared to ZnO TFTs, organic TFTs can be fabricated using very simple solution processing, which may provide a path to an inexpensive and simple to implement CMOS process.

There have been several previous reports of hybrid inorganic–organic CMOS processes. Katz et al. demonstrated CMOS inverters using amorphous silicon and α-hexathienylene TFTs fabricated on separate substrates, with field-effect mobility of <1 $cm^2/V\,s$ and <0.03 $cm^2/V\,s$, respectively [3]. Bonse et al. demonstrated ring oscillator circuits with a minimum propagation delay of 5 μs using a-Si:H and pentacene devices fabricated on a single substrate [4]. Low-voltage ZnO–pentacene CMOS circuits were demonstrated where both the ZnO and pentacene TFT mobilities were ~1 $cm^2/V\,s$, and a ZnO–pentacene inverter was shown to respond up to a 10 Hz input frequency with rise and fall times of 4 and 13 ms, respectively [5]. 5-stage hybrid CMOS ring oscillator circuits fabricated using indium gallium zinc oxide and pentacene TFTs operated with a minimum propagation delay of 1 ms/stage at 10 V [6]. All of the previous reports used vacuum-based processes to deposit the gate dielectric layer as well as both semiconducting layers. In addition, different metallization steps and pattering steps were required for the organic and inorganic semiconductor TFTs. These vacuum-based processes and additional mask steps result in a more complicated, expensive process. In addition to the complex processing, the dynamic performance of ZnO-based hybrid CMOS circuits thus far has been limited to >1 ms/stage. In this report we demonstrate a simple 4-mask CMOS process with bifunctional Ti/Au contacts and ZnO/organic hybrid circuits operating at <150 ns/stage at a supply voltage of 35 V.

We previously demonstrated a low-temperature (200 °C), atmospheric pressure, spatial atomic layer deposition process that allows rapid deposition (10–20 nm/min) of high-quality, uniform, and stable Al_2O_3 and ZnO thin films [7]. We have also demonstrated that these films can be used to fabricate high-mobility TFTs (>15 $cm^2/V\,s$) and fast ring oscillators (<31 ns/stage for 4 μm channel length) [8]. The fast circuits, good subthreshold slopes, and device stability are consistent with low interface state densities at the Al_2O_3/ZnO interface in these TFTs [7,8]. We have also previously reported that the organic semiconductor difluoro 5,11-bis(triethylsilylethynyl) anthradithiophene (diF TES-ADT) yields a different and more ordered microstructure on and near pentafluorobenzene-thiol-treated gold electrodes than on untreated oxide surfaces, resulting in high-mobility (~0.1–1 $cm^2/V\,s$) and a self-patterning character for diF TES-ADT TFTs and circuits [9,10]. The nature of this crystallization phenomenon and its impact on the electrical properties of the material and interfaces is related to contact treatments and molecular design and has been described in detail in several previous reports [9–12]. Using this self-patterning microstructure we demonstrated simple all-organic circuits operating at 3.3 μs/stage with no direct patterning of the organic layer [11]. We report here an integrated approach that combines these two technologies in a simple way to form high-speed, low-temperature CMOS circuits.

2. Experimental

The hybrid inorganic/organic CMOS circuits were fabricated on 2.5″ × 2.5″ borosilicate glass substrates, with an ion beam sputtered and photolithographically patterned chromium layer used for both the organic and inorganic TFT gates. Spatial ALD was used to deposit 150 nm of Al_2O_3 and 100 nm ZnO at 200 °C and atmospheric pressure. Photolithography and wet etching were used to pattern the ZnO and Al_2O_3 layers. Next, using a double-layer photoresist (Novalak/PMMA) mask, we first Ar ion beam-etched our ZnO contact surface and then deposited ion beam-sputtered Ti/Au (10/100 nm) and patterned electrodes by lift-off. The ion beam etching of the contact area improves the contact resistance to the ZnO [13]. Ti/Au was used because the Ti bottom layer makes a good contact to the n-channel ZnO and the Au top layer makes a good contact to the p-channel diF TES-ADT, minimizing the processing and mask steps required for device fabrication. The Ti/Au electrodes were then treated with the self-assembled monolayer pentafluorobenzene thiol (PFBT), and the Al_2O_3 dielectric was treated with hexamethyldisilazane (HMDS). The diF TES-ADT organic semiconductor was then spin-cast from a 2.5 wt.% solution in chlorobenzene with a chlorobenzene solvent vapor ambient maintained above the sample during spin-casting to promote uniform, large grain growth on and near the near the PFBT-treated contacts [14]. The solvent spinning combined with the contact-related microstructure previously mentioned is a straightforward way to achieve a highly controlled organic crystallization. The samples received a 30 min bake at 90 °C to remove residual solvent and were then tested. All devices and circuits were measured in air. A schematic cross-section and optical micrograph of a CMOS inverter and enlarged images showing the organic thin-film differential microstructure on gold and oxide are shown in Fig. 1. The differential microstructure between the treated gold electrodes and the untreated oxide areas provides enough device isolation for simple circuit operation without direct patterning of the organic semiconductor. The entire process required no vacuum processing to deposit the semiconducting and dielectric layers and only four masks and lithography steps.

3. Results

Discrete n-channel ZnO and and p-channel diF TES-ADT transistors were tested. The 150-nm-thick Al_2O_3 layer had a dielectric constant of eight. The n-channel ZnO transistors had mobility of 12–15 $cm^2/V\,s$ and threshold voltage of ~0–1 V. The p-channel diF TES-ADT transistors had mobility of ~0.1–0.2 $cm^2/V\,s$ and threshold voltage of ~8–12 V. In both transistors the off current was limited to ~1 μA due to residual leakage through the unpatterned organic layer and not through the ZnO layer which is fully